(11) LEVEL

DNA 4459F

UNDERGROUND DATA ACQUISITION AND TELEMETRY SYSTEM

DEVELCO, Inc.
404 Tasman Drive
Sunnyvale, California 94086

28 February 1977

Final Report for Period 10 June 1974—30 September 1976

CONTRACT No. DNA 001-74-C-0298

THIS WORK SPONSORED BY THE DEFENSE NUCLEAR AGENCY UNDER RDT&E RMSS CODES K400074462 J34DAXYX96901 AND K400076462 J34EAXYX96906 H2590D.

Prepared for

Director
DEFENSE NUCLEAR AGENCY
Washington, D. C. 20305

Destroy this report when it is no longer needed. Do not return to sender.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1 REPORT NUMBER DNA 4459F	2 GOVT ACCESSION NO	3 RECIPIENT'S CATALOG NUMBER
4 TITLE (and Subtitle) UNDERGROUND DATA ACQUISITION AND TELEMETRY SYSTEM	5 TYPE OF REPORT & PERIOD COVERED Final Report for Period 10 Jun 74—30 Sep 76 6 PERFORMING ORG. REPORT NUMBER 938-770228
7 AUTHOR(s) T. C. Moore, A. Weston L. H. Rorden, C. Kwong D. H. Nitta	8 CONTRACT OR GRANT NUMBER(s) DNA 001-74-C-0298
9 PERFORMING ORGANIZATION NAME AND ADDRESS DEVELCO, Inc. 404 Tasman Drive Sunnyvale, California 94086	10 PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS NWET Subtasks J34DAXYX969-01 and J34EAXYX969-06
11 CONTROLLING OFFICE NAME AND ADDRESS Director Defense Nuclear Agency Washington, D.C. 20305	12 REPORT DATE 28 February 1977 13 NUMBER OF PAGES 270
14 MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15 SECURITY CLASS (of this report) UNCLASSIFIED 15a DECLASSIFICATION DOWNGRADING SCHEDULE

16 DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17 DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18 SUPPLEMENTARY NOTES

This work sponsored by the Defense Nuclear Agency under RDT&E RMSS Codes K400074462 J34DAXYX96901 and K400076462 J34EAXYX96906 H2590D.

19 KEY WORDS (Continue on reverse side if necessary and identify by block number)

Underground Communication
Earth Motion Instrumentation
Shock Hardened Electronics
EM Propagation in a Lossy Medium

20 ABSTRACT (Continue on reverse side if necessary and identify by block number)

Three DEVELCO Underground Telemetry Systems were installed as part of the DNA Mighty Epic Nuclear Test Event interface experiment on 12 May 1976. These systems were designed to withstand strong shock and high pressures in order to acquire, store, and later telemeter multiple channels of ground motion data from high stress regions at depths greater than 1500 feet without relying on signal cables through the interface zone. In addition to recording significant new data, the Mighty Epic operation demonstrated that data storage and retrieval can be successfully accomplished under severe environmental conditions.

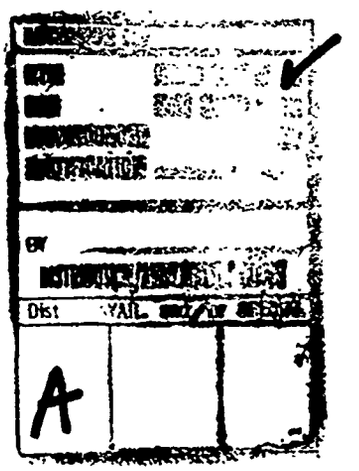
DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

SUMMARY

Three DEVELCO Underground Telemetry Systems were installed as part of the DNA Mighty Epic nuclear test event interface block motion experiment on 12 May 1976. These systems were designed and constructed to withstand strong shock and high pressures in order to acquire, store, and later telemeter, via low frequency electronic waves, multiple channels of ground motion data from depths greater than 1500 feet (500 meters) without relying on signal cables through the interface zone to the surface. All units survived the shock EMP and pressure caused by the nuclear explosion. All units operated properly after the test. One unit contained high quality data including significant late time information. The other two units did not contain ground motion data although they appear to have operated properly. This lack of valid ground motion data probably resulted from post shot retriggering of command acquisition cycles due to shorts created by massive cable failure. Future systems should incorporate command codes to prevent the recurrence of this problem. In addition to recording significant new data, the Mighty Epic operation demonstrated that data storage and retrieval can be successfully accomplished under severe environmental conditions and, transmitted through the earth to a receiver and data recorder on the surface. The techniques developed during this program are viable for similar applications in the future.



PREFACE

This work was sponsored by the Defense Nuclear Agency under RDT&E RMSS Code K400076462J34EAXYX96906H2590D and was performed under Contract Number DNA 001-74-C-0298.

The successful completion of this work was aided by many organizations associated with the Defense Nuclear Agency and the Nevada Test Site. Mr. Don Williams and Mr. Bob Workhoven and their associates at Sandia Laboratories, Albuquerque, provided valuable assistance on high shock packaging and testing, respectively. Mr. Harlan Aslin of Physics International was very helpful on EMP considerations and testing. Dr. Rey Shunk, Electromechanical Systems of New Mexico, Dr. Bruce Hartenbaum, H-Tech, and Dr. Victor VanLint provided valuable experience and guidance in their role as DNA consultants. Mr. Don Day and his staff at the Waterways Experiment Station did an excellent job of fielding the equipment under severe time constraints. Special credit must be given to the Mighty Epic Technical Director, LTC Herb Ellis, and his associates, LCDR's Lee Piper and John Gallamore, at DNA Field Command, for outstanding leadership and direction on this very difficult program.

CONTENTS

1. INTRODUCTION

The data acquisition and underground telemetry systems described in this report were designed to acquire earth motion data from sensors located very near and below underground nuclear explosions. The systems were used in the Defense Nuclear Agency (DNA) Interface Experiment of the Might Epic event conducted on 12 May 1976 at the Nevada Test Site. The experiment was originally designed to be a part of the DNA Minty Delight event with prototype tests on Husky Pup. Changes in DNA plans precluded the deployment of this experiment on these events. The primary purpose of the experiment was to determine the explosion's effects, such as relative motion, on stratified rock environments using a large number of hardened ground motion detectors. The problem in trying to retrieve such data is that very high stress levels and large differential motions exist which preclude the use of conventional cable techniques. Inaccessible borehole locations make the cost of recovery systems prohibitive.

Although progress has been made in utilizing hardened cables in some applications, cables will not survive when they must pass through the working point and are unlikely to survive when they pass through transitions between stratified media. Thus, the data must be transmitted through the earth from these inaccessible locations. This can be accomplished with relatively short, hardened canisters that are designed to survive the severe stress environment. Seismic methods are not practical due to difficulties in coupling signals into the earth from boreholes and the relatively high attenuation rates at the frequencies required for the transmission of data. Electromagnetic (EM) methods are tractable although they also suffer range and bandwidth limitations due to the earth's conductivity.

Previous EM telemetry systems designed and constructed by Develco, such as that used on the Defense Atomic Support Agency (DASA) Discus Thrower event in 1966 and other applications,[1,2,3] have demonstrated the feasibility of transmitting data through the earth. These early systems utilized relatively high frequencies (kilohertz) to transmit data in real time from a limited number of gauges (one to three) over distances of several hundred meters.

Data channel bandwidths were relatively narrow (less than 2 kHz) and earth conductivity conditions ranged from favorable to moderate. Data were transmitted either to the surface, via repeaters, or to a receiver in an adjacent borehole where the cable would survive.

The current experiments required relatively wide bandwidths approaching 10 kHz from numerous transducers (20 to 40 total) of varying types at several locations. Thus, the number of channels and bandwidths were greater than the propagation conditions could support for real-time transmission without an excessive number of repeaters which would have a large impact on reliability and cost. The need for more elaborate techniques to compensate for antenna motion during ground shock was also a factor. These considerations precluded the utilization of real-time transmission which was used in previous experiments. Thus, a concept evolved[4,5] which used storage of the wide bandwidth data in hardened canisters during the event and transmission of the data at low rates many hundreds of meters to the surface after the event.

2. UNDERGROUND TELEMETRY SYSTEM DESCRIPTION

2.1 SYSTEM CONFIGURATION

Three Develco Underground Telemetry Downhole Units, Figure 2.1-1, were installed as part of the Interface Experiment, fielded by the U.S. Army Engineer Waterways Experiment Station (WES), on the Mighty Epic event of 12 May 1976. The downhole units, designed to withstand pressure and shock in excess of 1 kilobar (10^5 kPa) and 3000 G, respectively, were positioned below the tuff/quartzite interface approximately as shown in Figure 2.1-2. Each unit was connected to 12 external stress, acceleration, or velocity gauges, supplied by WES, for collecting data at wide bandwidths (up to 10 kHz) during the event. The data was then converted to digital form and stored until recalled by command days or weeks later.

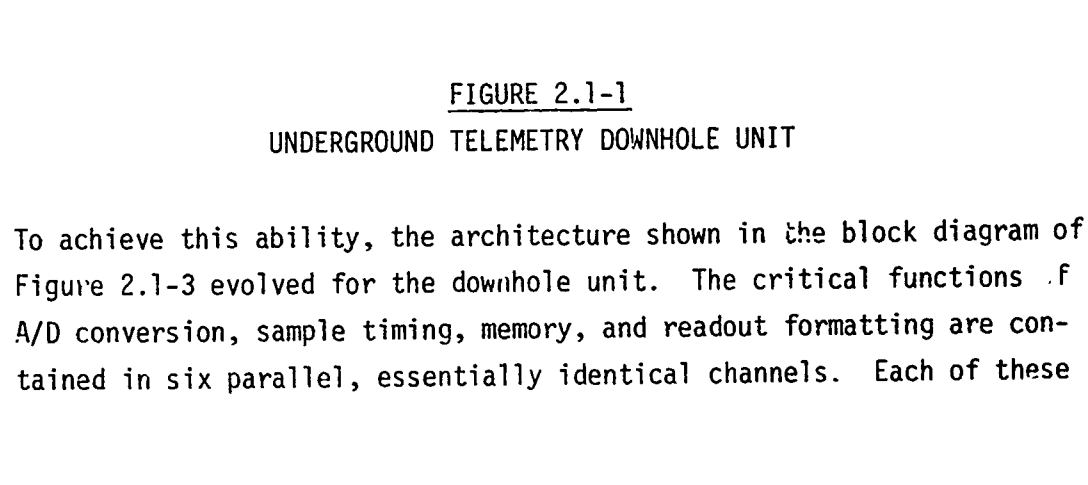


FIGURE 2.1-1
UNDERGROUND TELEMETRY DOWNHOLE UNIT

To achieve this ability, the architecture shown in the block diagram of Figure 2.1-3 evolved for the downhole unit. The critical functions of A/D conversion, sample timing, memory, and readout formatting are contained in six parallel, essentially identical channels. Each of these

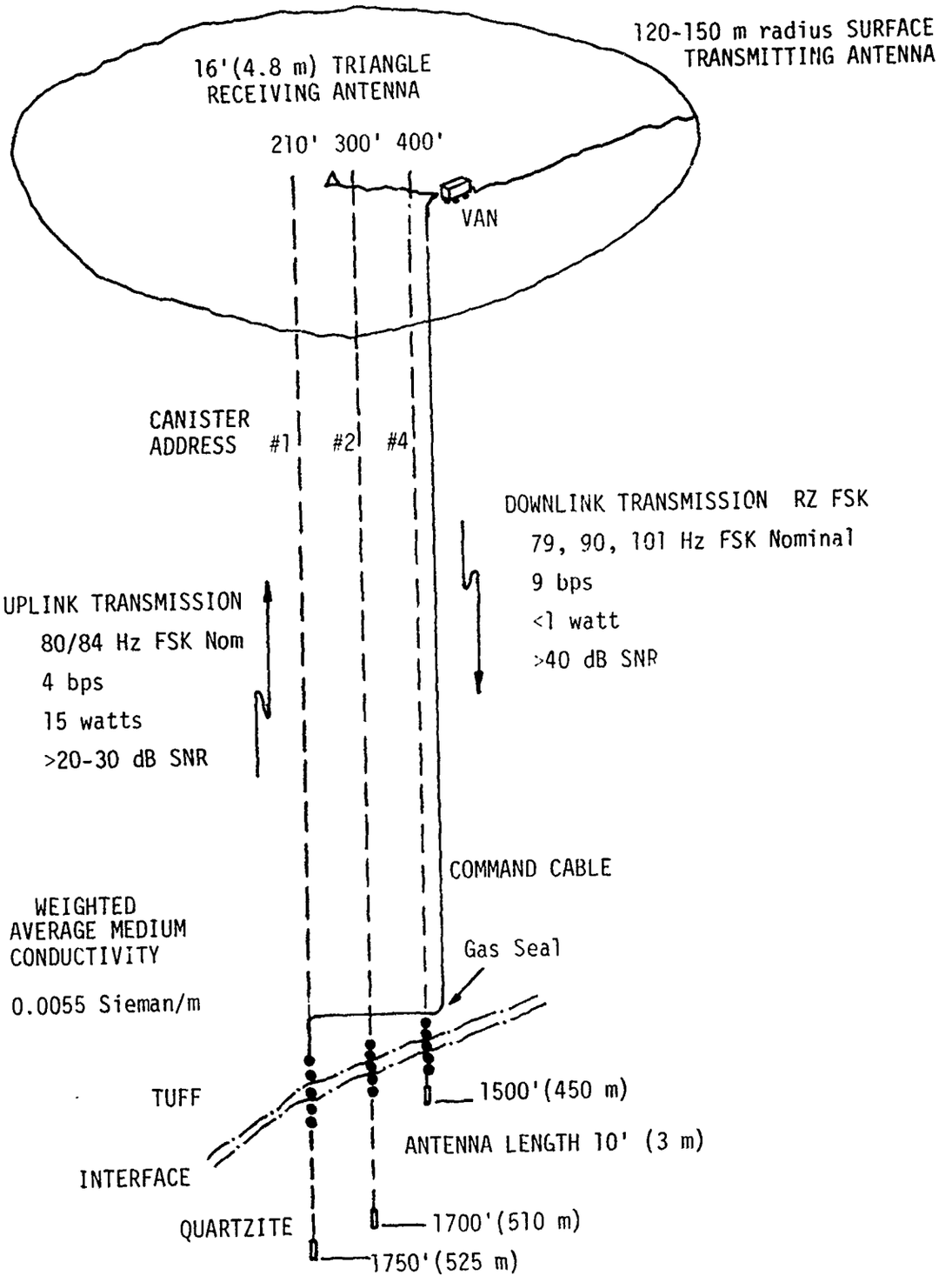


FIGURE 2.1-2

MIGHTY EPIC UNDERGROUND TELEMETRY SYSTEM CONFIGURATION

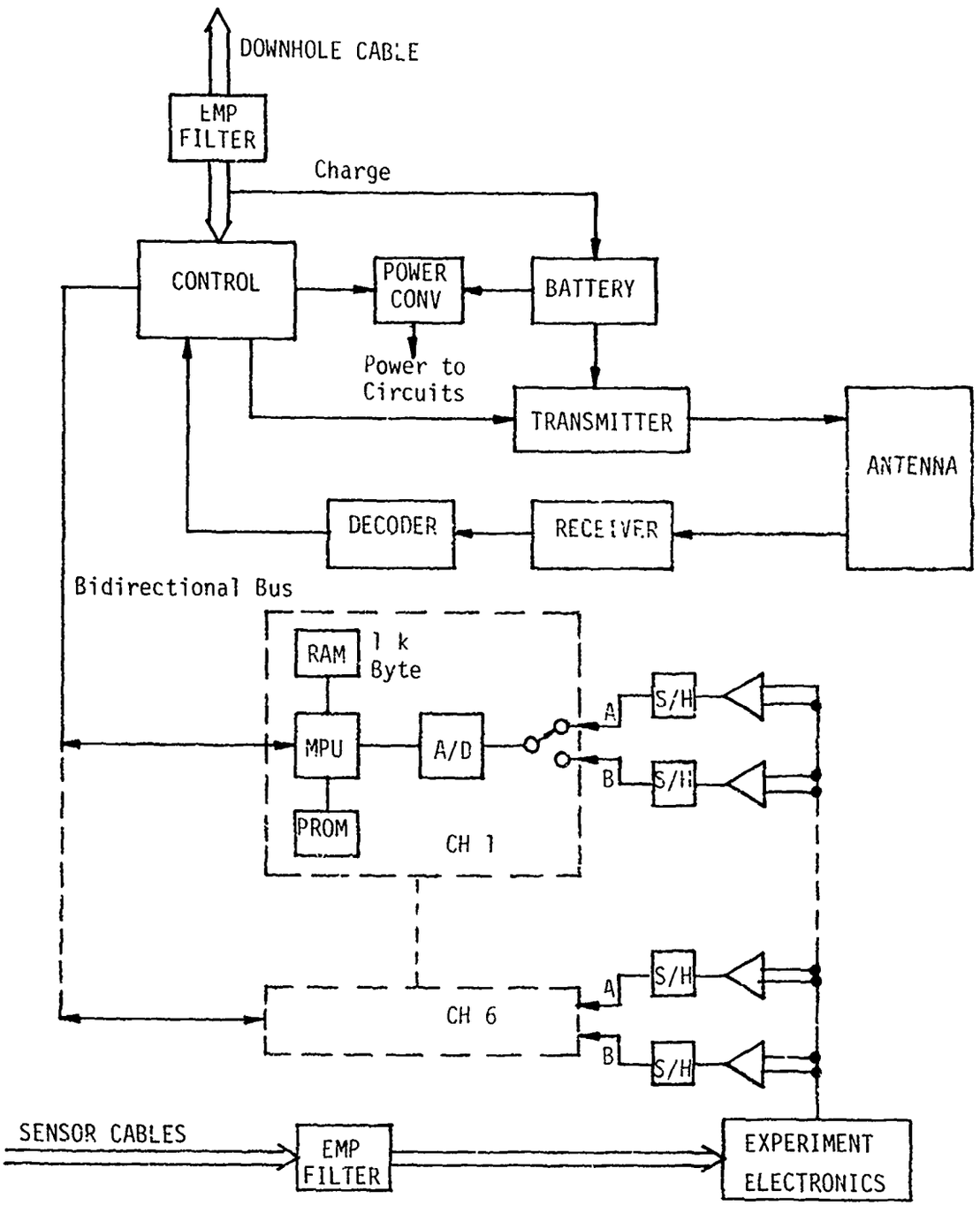


FIGURE 2.1-3

DOWNHOLE UNIT BLOCK DIAGRAM

channels contains a separate microprocessor unit (MPU), can multiplex inputs from two sensors, can be programmed to take data samples with wide flexibility, will format data readouts in addressable blocks by command, will verify commands before responding, and insert housekeeping data in each readout for system performance evaluation. As shown in the block diagram, these MPU channels are linked by a common bidirectional bus to a control circuit which determines the mode of operation of the canister by applying power to the appropriate converters and MPU channels.

Wellhead (i.e., surface) equipment, Figure 2.1-4, is used to turn on, monitor, charge batteries, and initiate the data acquisition process in the downhole units through cables prior to the event. When the downhole unit is turned on, it is in the standby mode with only the data memories, command receiver and decoder operating. The power drain of 40 to 80 milliwatts is less than the internal leakage of the 10^6 joule (approximately 280 watt-hours) Nicad battery in this mode. A Ready signal on the downhole cable turns on all six MPU's and a high-power converter, enabling the Acquisition mode. Receipt of a FIDU signal on the downhole cable starts the timeout of each channel for data sampling according to its programmed sequence, which cannot be interrupted or stopped by any signal. Not until 30 seconds after acquisition starts, when the system reverts to standby, is it possible to initiate either a new acquisition or a readout cycle.

The wellhead equipment is also used to transmit downlink data dump commands to, and receive uplink data messages from, the downhole units through surface antennas after the event. Thus, the third mode, Transmit, is initiated by receipt of a valid command, which causes one of the six addressable MPU's to be turned on. This MPU then verifies that the correct preamble, canister address, and MPU address have been received; if not, it resets the system to standby. If the command is valid, the MPU accepts the rest of it, which calls out the bit rate, first data block to be transmitted, and number of data blocks to be transmitted. A data block consists of eight bytes (samples of 8 bits each), and readout may commence with any block in the 1000-byte (125 block) channel memory. The MPU then turns on the transmitter, and encodes the preamble, 3 bytes of housekeeping, and the data blocks requested, then returns the system to standby.

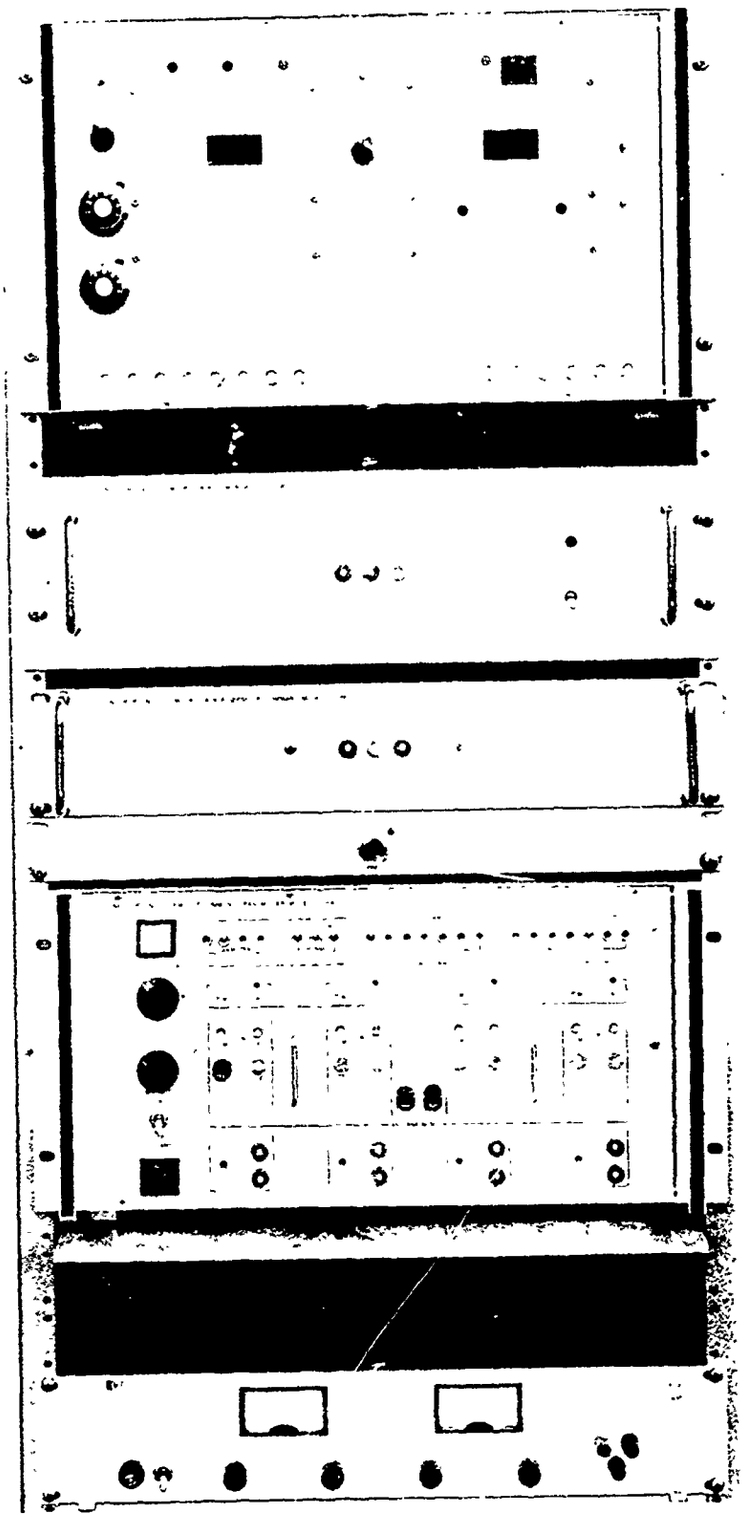


FIGURE 2.1-4

WELLHEAD EQUIPMENT

To minimize the required memory capacity, data sampling times can be programmed as illustrated in Figure 2.1-5, superimposed on a typical ground motion signal. A timeout delay after FIDU can be specified for the first data sample. Samples can then be taken at short intervals over the signal rise time, which is generally short; then successively longer and longer intervals as the transient decays, thereby achieving both high resolution when it is needed, and long duration when the resolution is not important.

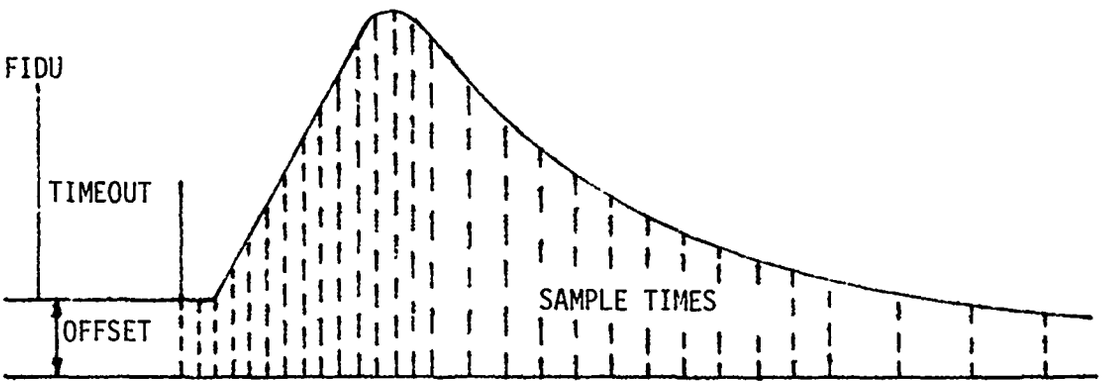


FIGURE 2.1-5
DATA SAMPLING ILLUSTRATION

An unusual aspect of the data acquisition architecture is the use of 10-bit A/D conversion, with storage and readout of only the lower 8 bits. This allows the signal to overrange the nominal conversion window by a factor of four without saturating or even losing accuracy. Since data samples are points on a continuous function, the lost two bits can be recovered by continuity. That is, an overranging signal will appear, on readout, to jump from full scale to zero (or conversely) and continue to trace the signal. It is obvious on inspection of the readout, as in Figure 2.1-6, that continuity is restored at this point by adding the next higher bit value to the data. This figure, which shows a test readout of a triangle wave signal biased to overrange on each cycle, also illustrates the effect of changing sample rate.

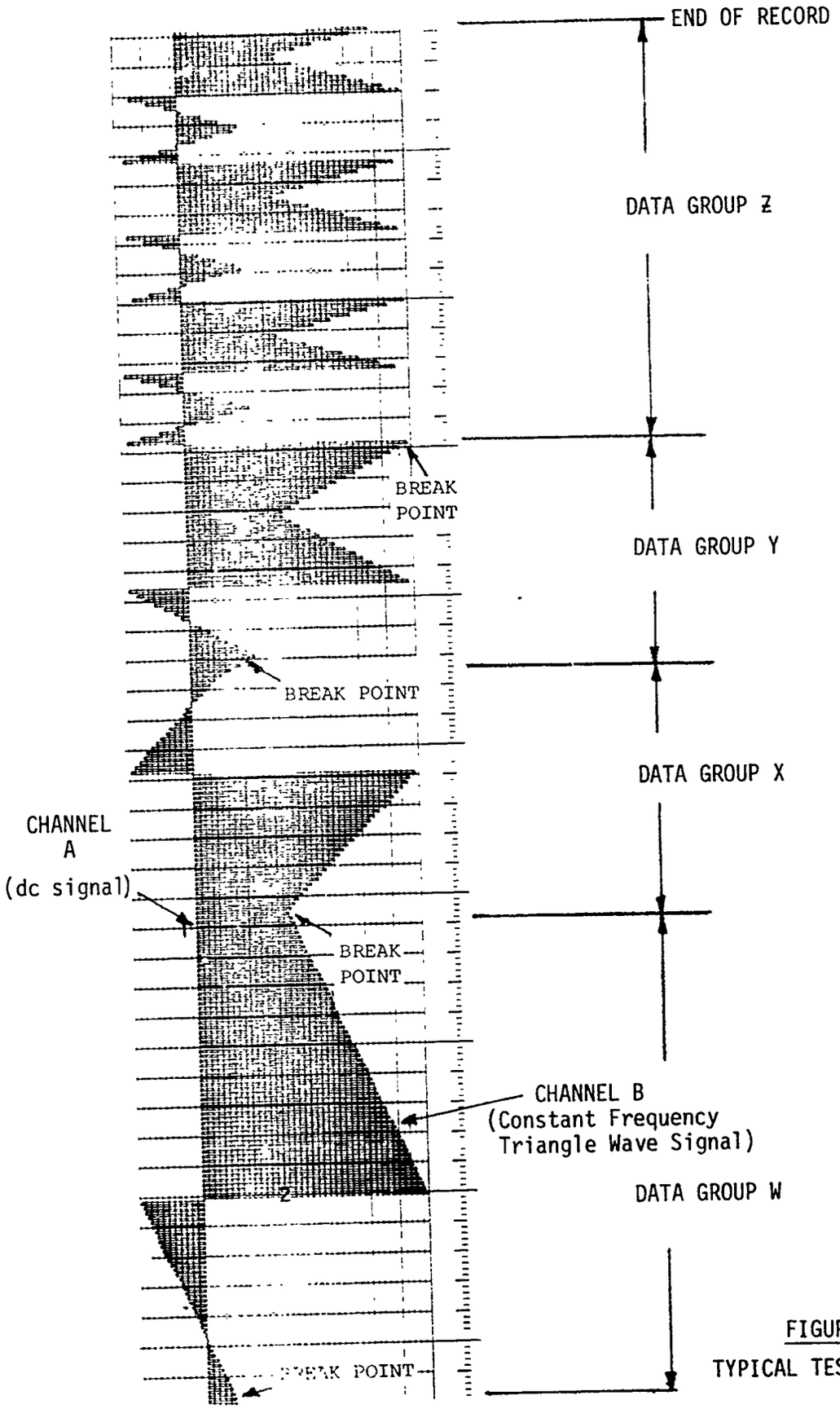


FIGURE 2.1-6

TYPICAL TEST DATA SAMPLE

For survival in the severe environment, the system was packaged as shown in Figure 2.1-7. Electronics are [illegible] circular boards with circular aluminum compression rings bonded to them. Components are conformal coated and foamed with high-density (12-20 lb/ft^3 or 190 to 320 kg/m^3) urethane foam and then faced off to exact height. A number of these wafers are stacked into a module as shown, and loaded in compression by high-strength bolts through the stack. Each wafer is shock tested to 3000 g's before assembly. Board-to-board wiring is accomplished by inserting wires of appropriate length in pin sockets around the periphery of each board. The ends are crimped to prevent the wires from pulling out during shock. Molded MDM connectors carry the stack wiring from module to module, through the captured bulkheads that restrain motion of the stacks in the canister. Downhole Unit system specifications are summarized in Table 2-1.

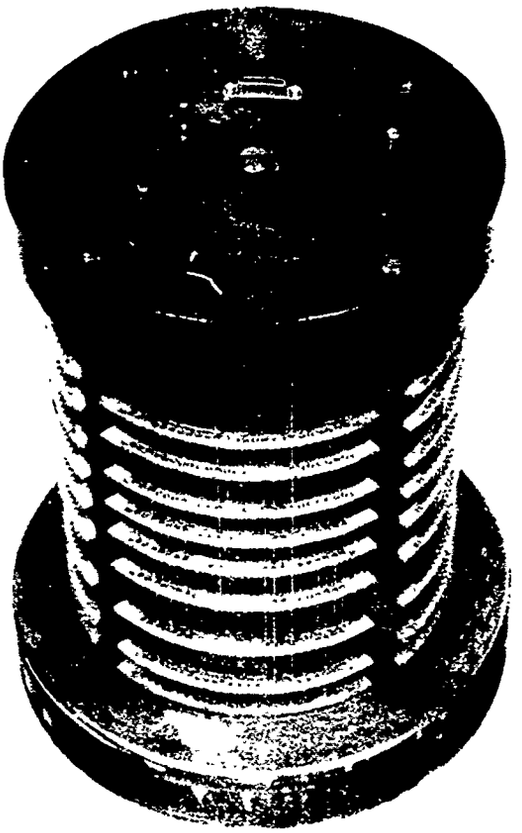


FIGURE 2.1-7
DOWNHOLE UNIT ELECTRONICS MODULE

TABLE 2-1

SYSTEM SPECIFICATIONS

ACQUISITION	External Sensors	12
	Bandwidth	10 kHz
	Digital Resolution	8 bits
	Overrange	times 4
	Maximum Sample Rate per Channel	19,000/second
	Maximum Sample Rate Supercommutated	38,000/second
STORAGE	Memory Capacity per Channel	500 samples
	Storage Time to 2 Memory Dumps	Greater than 15 days
	Storage Time to 1 Memory Dump	Greater than 30 days
SIGNAL INPUT INTERFACE	Channels (2-wire differential)	12
	Maximum Input Voltage	±25 V
	Maximum Differential Input Voltage	±10 V
	Input Impedance (CM or differential)	Greater than 25 kilohms
	Common Mode Rejection	Greater than 34 dB
	Gain Accuracy	±2½%
	Analog Bandwidth (excluding EMP fltr)	16 kHz
	Digital Span (8 bits)	5 V
	Digital Resolution	0.0195 V
READOUT	Data Rate	4 bits/second
	Time for Memory Dump	Less than 5 hours
	Error Detection	1 parity bit per sample
	Minimum Block	8 samples
MECHANICAL	Length	22 feet (6.6 m)
	Maximum Diameter	11 inches (28 cm)
	Weight	2400 lbs (1080 kg)
ENVIRONMENT	Maximum Stress	1 kilobar (10^5 kPa)
	Maximum Axial Shock	3000 G
	Maximum Lateral Shock	1000 G

2.2 MICROPROCESSOR, MEMORY AND DIGITAL SYSTEM

This section describes the digital system, including the MPU and the software programs. The operation of the system is included along with a description of the circuit boards.

Excerpts from Motorola's M6800 Microprocessor Application Manual have been included to briefly familiarize the reader with Motorola's Microprocessing Unit (MPU) MC6800 and its family of devices and, in particular, the Peripheral Interface Adaptor (PIA) MC6820. For more details, the reader is referred to the application manual mentioned above the data sheets for the MPU-MC6800, PIA-MC6820, and two other parts required to make a microcomputer family - namely, memories PROM-MF1702AR and RAM-1M6508.

2.2.1 Introduction to the MC6800 Microprocessor

Motorola has elected to provide a microprocessor family of parts headed by the MC6800 Microprocessing Unit. The MC6800 MPU is an eight-bit parallel microprocessor with addressing capability of up to 65,536 words. It is Transistor-Transistor Logic (TTL) compatible, requiring only a single 5-volt supply and no external TTL devices for bus interface in small systems.

In support of the MPU are several memory and I/O interface devices. To date, the family consists of a 128 x 8 Random Access Memory (RAM) (MC-6810), a 1024 x 8 ROM (MCM6830), a parallel I/O interface (MC6820 PIA), and an asynchronous serial I/O interface (MC6850 ACIA). In keeping with the family concept, each operates on a single 5-volt power supply and is compatible with the system bus signals. The family of parts is not a chip set in the sense that the MPU operation is dependent upon other family elements; the MC6800 is a self-contained microprocessor capable of operating with virtually any Metal Oxide Semiconductor (MOS) or standard TTL device. The significant point is that the other family members merely add additional capability and/or flexibility. They provide excellent tools in configuring a full microprocessor operating system.

2.2.1.1 System Organization

Before describing the individual parts in any detail, an explanation of the MPU bus and control structure will serve to demonstrate how a system is brought together. Figure 2.2-1 is organized to show the processor's inputs and outputs in four functional categories; data, address, control, and supervisory.

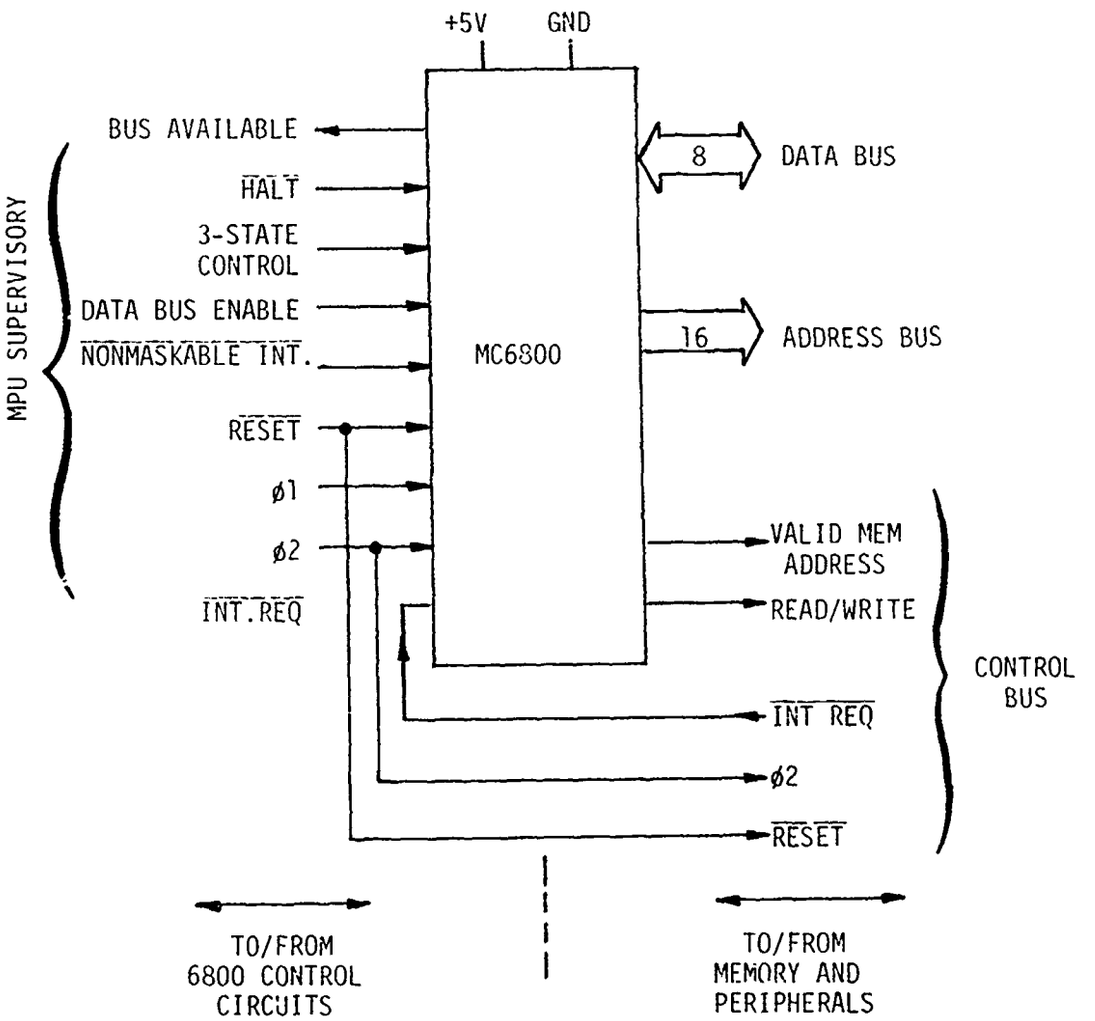


FIGURE 2.2-1

MC6800 BUS AND CONTROL SIGNALS

The width and drive capability of the Data Bus has become a standard means of measuring microprocessors. The MC6800 has an 8-bit bidirectional bus to facilitate data flow throughout the system. The MPU Data Bus will drive up to 130 pF and one standard TTL load. As a result of the load characteristics of the RAM, ROM, ACIA, and PIA, the MPU can drive from 7 to 10 family devices without buffering.

Using the family I/O interface devices allows the 16-bit Address Bus to assume additional responsibility in the M6800 system. Not only does the Address Bus specify memory, but it becomes a tool to specify I/O devices. By means of its connections to the Data Bus, Control Bus, and selected address lines, the I/O interface is allocated an area of memory. As a result, the user may converse with I/O using any of the memory reference instructions, selecting the desired peripheral with a memory address.

In addition to the Data and Address Bus, a Control Bus is provided for the memory and interface devices. The Control Bus consists of a heterogeneous mix of signals to regulate system operation. Following is a brief review of the designated Control Bus signals shown in Figure 2.2-1. ø2 is one phase of the system clock applied to the MPU. It is applied to the enable or chip select inputs of the family parts to insure that the devices are enabled only when the address bus and VMA are stable. $\overline{\text{Reset}}$ is used to reset and start the MPU from a power down condition. It is also routed to the $\overline{\text{Reset}}$ inputs of the PIA's for use during power on initialization. $\overline{\text{Interrupt Request}}$ is generated by the PIA, ACIA, or user-defined hardware to notify the MPU of a request for service.

Read/Write (R/W) and Valid Memory Address (VMA) are MPU outputs characterizing the Data Bus and Address Bus, respectively. R/W designates whether the MPU is in a Read or Write mode for each cycle. VMA indicates to memory and I/O that the MPU is performing a read or write operation in a given cycle. This signal is applied to the enable or chip select inputs of each family device in order to disable data transfer when VMA is low.

The last set of signals in Figure 2.2-1, the MPU Supervisory, is used for timing and control of the MC6800 itself. Note that three of the Supervisory signals are shared with the Control Bus and affect the memory and I/O devices as well.

ø1 is one of the two clock phases to the MPU. $\overline{\text{NonMaskable Interrupt}}$ ($\overline{\text{NMI}}$) is similar to the interrupt request input mentioned earlier, except that $\overline{\text{NMI}}$ will always be serviced regardless of the state of a programmable interrupt mask contained within the processor. Data Bus Enable (DBE) is the three-state control signal for the MPU Data Bus. Normally, this signal will be ø2, derived from the clock. Three-state control (TSC) affects the Address Bus and the R/W line in the same manner that DBE controls the Data Bus. This signal can be used, for example, to accomplish a direct memory access by putting the Address Bus and the R/W line in the high impedance state. The last supervisory input is the $\overline{\text{Halt}}$ signal. When $\overline{\text{Halt}}$ is low, the MPU will stop processing. In the $\overline{\text{Halt}}$ mode, all three-state signals will be in a high impedance state (address, data and R/W), VMA will be low, and Bus Available will be high.

The Bus Available supervisory output from the MPU is normally in an inactive low state. It is brought high by the occurrence of the $\overline{\text{Halt}}$ input low or by execution of a WAIT instruction. In either case, the MPU stops program execution and sets Bus Available hign, indicating that all the three-state buffers are in the high impedance state. If the MPU has stopped as a result of the $\overline{\text{Halt}}$ signal, Bus Available will remain high until the $\overline{\text{Halt}}$ input is again taken high. If the MPU has stopped as a result of the WAIT instruction, it is waiting for an interrupt and Bus Available will remain active until a non-maskable interrupt or interrupt request occurs. Bus Available may be used to signal external hardware that the MPU is off the bus for multiprocessor or direct memory access applications.

2.2.1.2 M6800 Family Elements

With the MC6800 as the focal point, a variety of memory and I/O devices may be tied onto the bus network. The busses will provide TTL compatible voltage levels (V_{OH} = 2.4 V, V_{OL} = 0.4 V) while driving capacitive loads up to 130 picofarads with current loads of up to 1.6 mA sink current and 100 μA source current.

Memory on the bus - Memory is connected in a straightforward fashion by tying directly to the MC6800 busses. Block diagrams of the RAM and PROM are shown in Figures 2.2-2 and 2.2-3, respectively. Notice that the data lines have three-state buffers permitting the memory data signals to wire-OR directly onto the system data bus. The enable input, when active, selects the specified device as defined by the address inputs. For a small to medium size system, no additional address decoding is necessary. The memories are TTL compatible. Static operation eliminates the need for clocks or refresh.

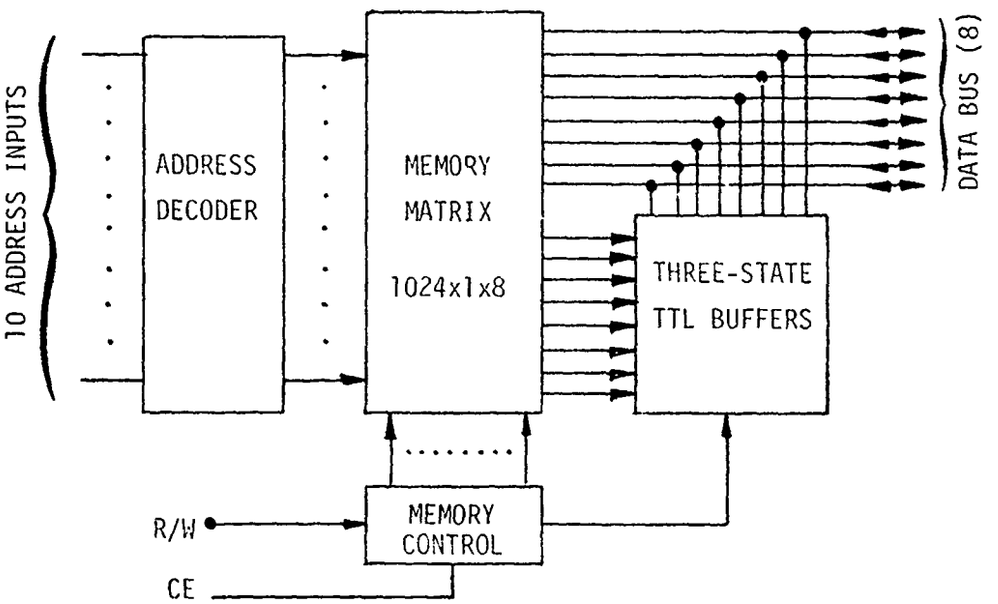


FIGURE 2.2-2
RAM FUNCTIONAL BLOCK DIAGRAM

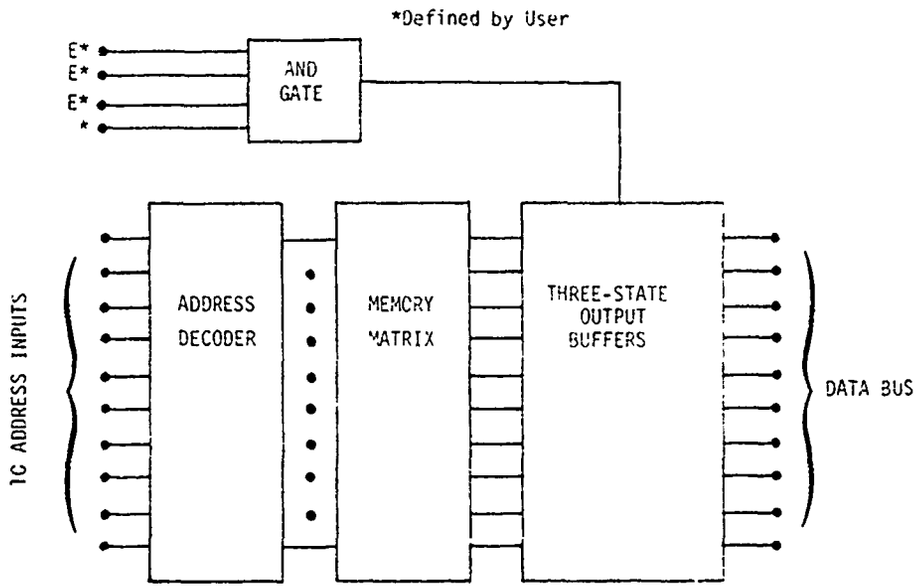


FIGURE 2.2-3
PROM FUNCTIONAL BLOCK DIAGRAM

I/O on the Bus - The family I/O devices are also tied directly to the bus network. In the M6800 architecture, I/O is configured to respond to MPU instructions in the same fashion as memory. This is accomplished by tapping off the MPU busses such that I/O has a "memory" address that the MPU references. Two devices available for interfacing the microprocessor with the outside world are the MC6820, Peripheral Interface Adaptor (PIA), for parallel interface, and the MC6850, Asynchronous Communication Adaptor (ACIA), for serial interface. Both are designed to tie directly to the MPU busses and transfer signals between peripherals and the MPU under program control.

Interfacing the MPU to a variety of I/O devices is straightforward with the PIA. It is a programmable general purpose parallel interface device

designed to interface the MPU to peripherals through two 8-bit bidirectional peripheral data busses and four control lines as shown in Figure 2.2-4.

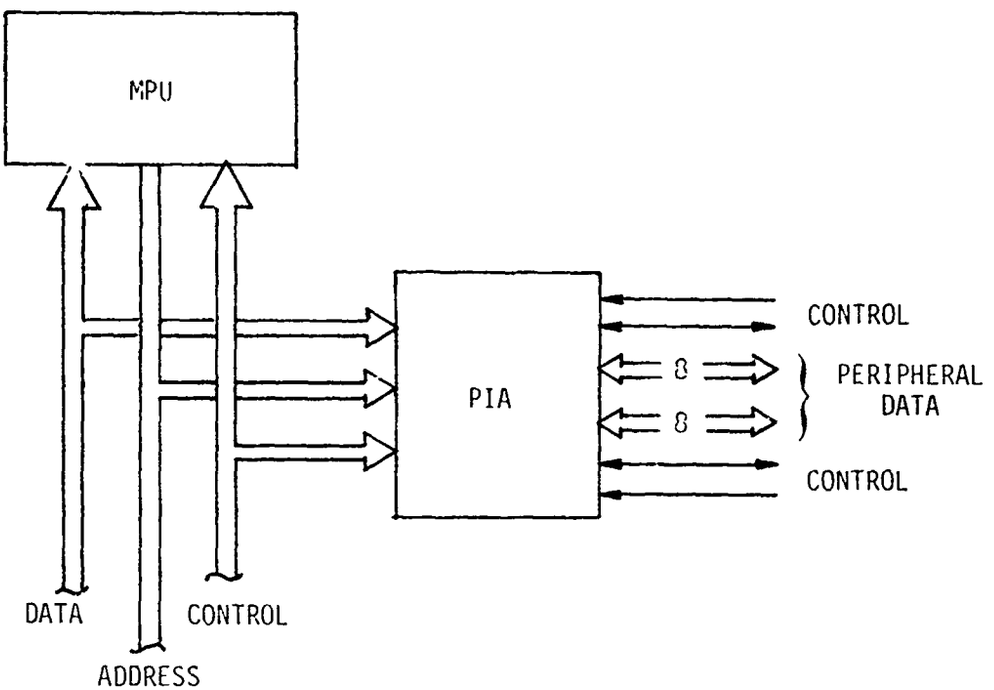


FIGURE 2.2-4
MPU PARALLEL I/O INTERFACE

The MPU/PIA interface consists of three elements: 8 data lines, 5 address lines, and 5 control lines (see Figure 2.2-5). The data lines are bidirectional common to the MPU data bus. The PIA taps off 5 bits from the 16-bit MPU address bus. These 5 inputs are utilized to select the PIA (CS0, CS1, $\overline{CS2}$) as well as registers within the PIA (RS0 and RS1). The PIA uses all of the signals on the MPU control bus. The R/W input ties directly to the MPU R/W output to control direction of data flow. The PIA has two independent Interrupt Request outputs that may be wire-ORed together and tied to the $\overline{IRQ}$ line of the control bus or applied separately to prioritizing circuitry. The $\overline{Reset}$ input may

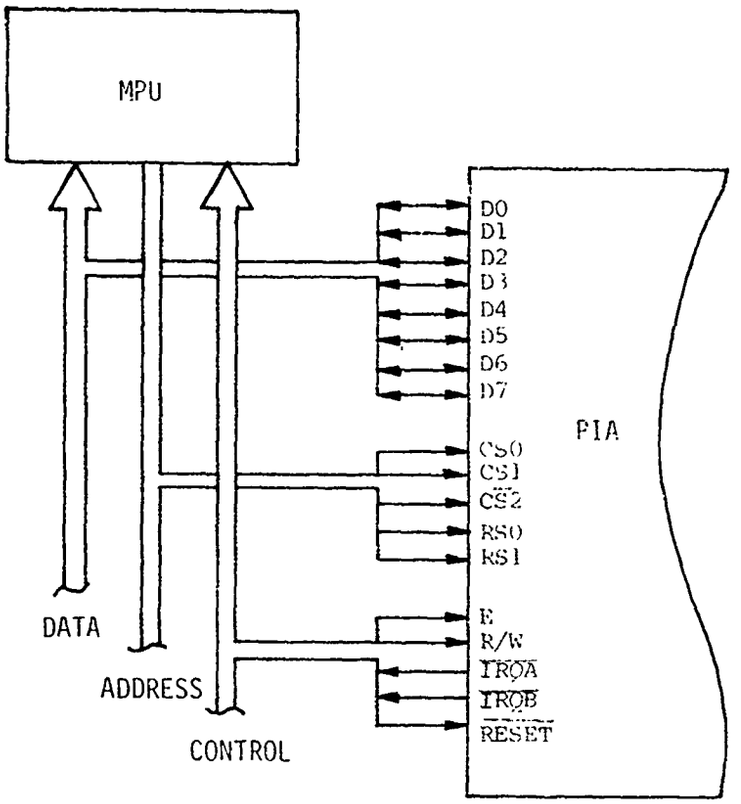


FIGURE 2.2-5
MPU/PIA INTERFACE

be tied directly to the MPU control bus to initialize the PIA to an all zero condition when required. Finally, the Enable input is the timing signal to be supplied to the PIA. This input is typically the ø2 clock.

The PIA is programmable in the sense that the MPU can read and/or write into its internal registers. There are a total of six 8-bit registers in the PIA. They are separated into an A and B side, each side containing a Control Register, Data Direction Register, and an Output Data Register (Figure 2.2-6). To define operation of the PIA control lines, an 8-bit word is loaded into the Control Register. Likewise, to define the PIA/peripheral data lines to be inputs or outputs, an 8-bit word is loaded into the Data Direction Register. Finally, data being transferred to peripherals may be saved in the PIA Output Data Register.

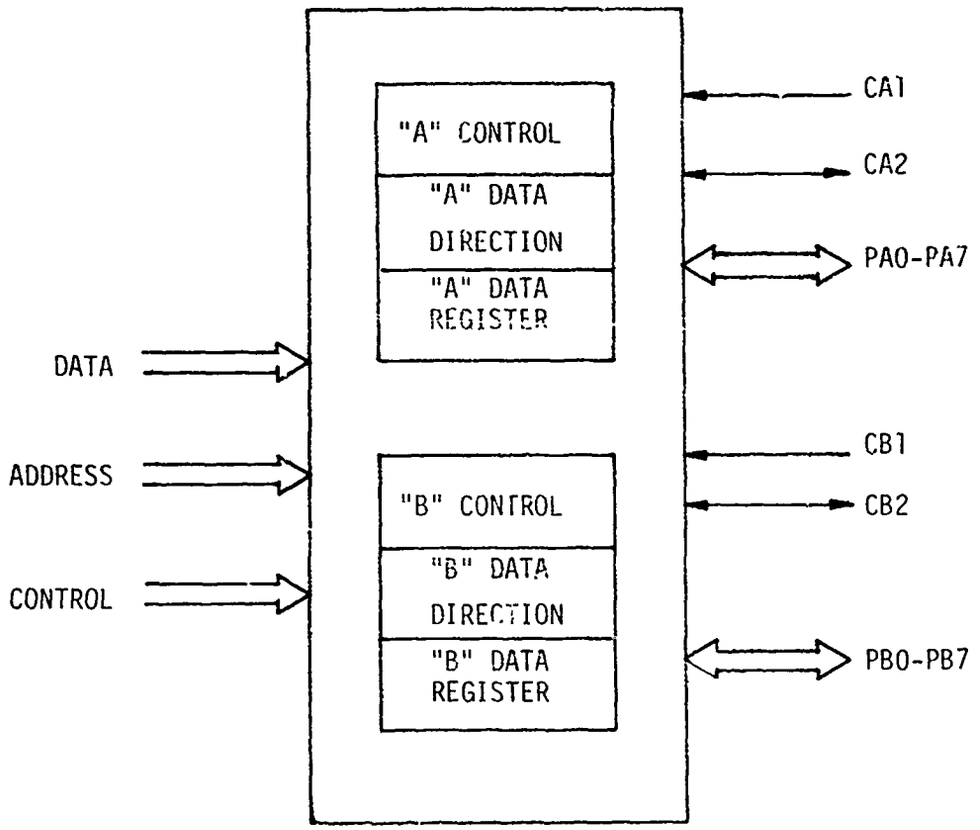


FIGURE 2.2-6
PIA REGISTERS

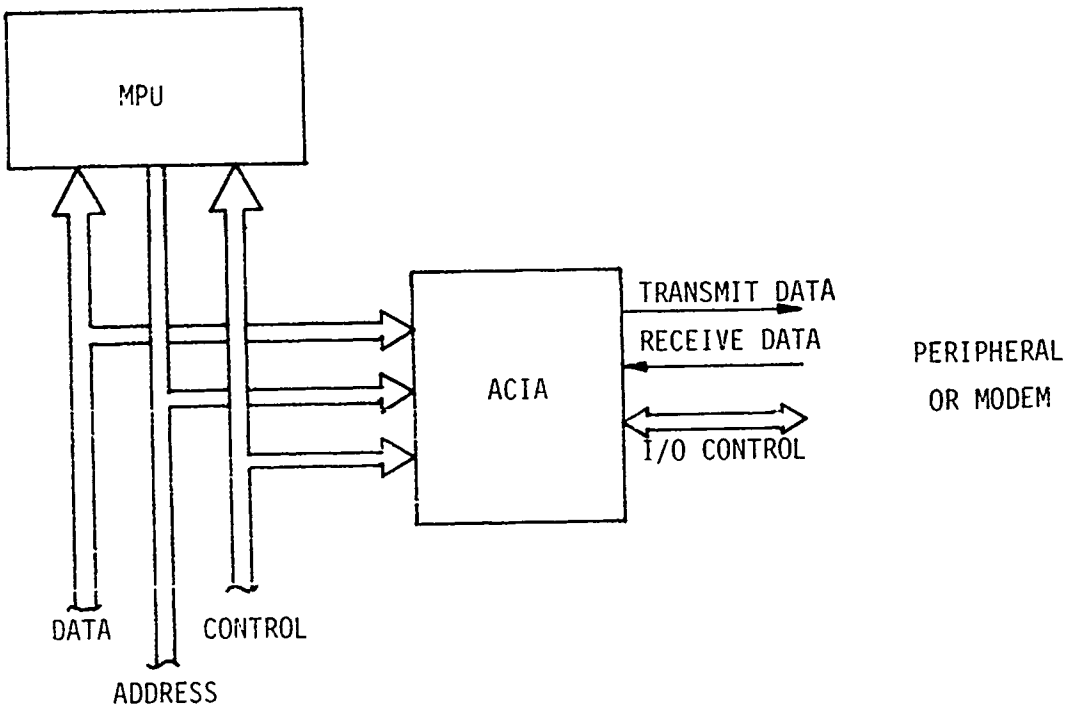


FIGURE 2.2-7

MPU SERIAL I/O INTERFACE

2.2.2 Digital System Operation

Figure 2.2-8 is a block diagram of the digital section at the PC board level. There are two basic modes of operation: (a) Data Acquisition, and (b) Data Transmission. This section describes these modes in terms of the PC boards and the block diagram.

2.2.2.1 Data Acquisition Mode

To initialize the acquiral mode, a Ready signal is required which goes to the Control and Timing board to make I/O 7 go high and turn on the power supplies. This I/O 7 line goes to the Input board of the memory section which tests the line. If I/O 7 is high, the system knows it is in the acquiral mode. It will wait for a FIDU signal which also goes to the Control and Timing board to make I/O 6 go high. This I/O 6 line goes to the Input board and is tested. If I/O 6 is high and I/O 7 is still high, then the memory will execute the acquiral program.

When the Ready signal is received, the power supplies will turn on and stay on (assuming a proper FIDU signal was received) for two seconds after this FIDU signal. During this time, data is acquired and stored in the RAM. Thirty seconds after the FIDU signal, the system will go into a standby mode. In standby mode, only the RAM board, Control and Timing board and the two Command Receiver-Decoder boards are on (+5V S standby power).

During acquiral, the 12 sensor data lines go to 6 Input boards (each board multiplexes two sensors) which digitize the analog data into 8 bits and store the data in the RAM board for each channel. The microprocessor uses the information in the PROM's to determine the sampling rates and where to store the input data. Refer to the software section for descriptions of the various programs. Housekeeping data is also processed during the acquiral mode.

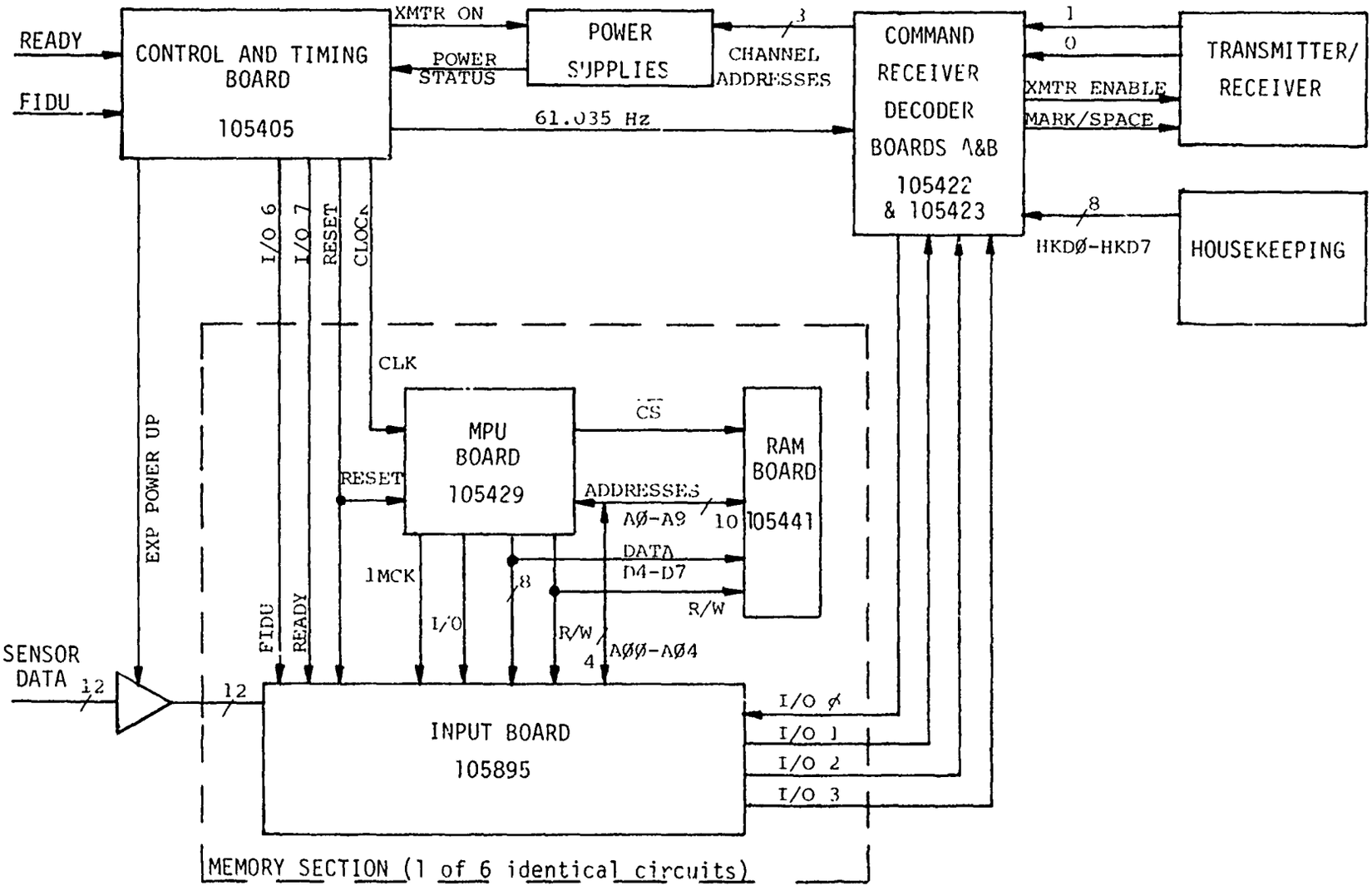


FIGURE 2.2-8

DIGITAL SECTION BLOCK DIAGRAM

2.2.2.2 Data Transmission

To initialize the transmit mode, I/O 7 on the Control and Timing must be low. A data acquiral mode is required before a transmit mode can occur; during the acquiral mode I/O 7 is eventually set to a low state and stays low after the acquiral mode has completed its cycle (the system goes into its standby mode). The low state of I/O 7, which goes to the Input board, signals the memory section that it is in the transmit mode. The MPU cannot test this flag until the power supplies for the selected canister and channel MPU have been turned on by the Command Receiver Decoder board.

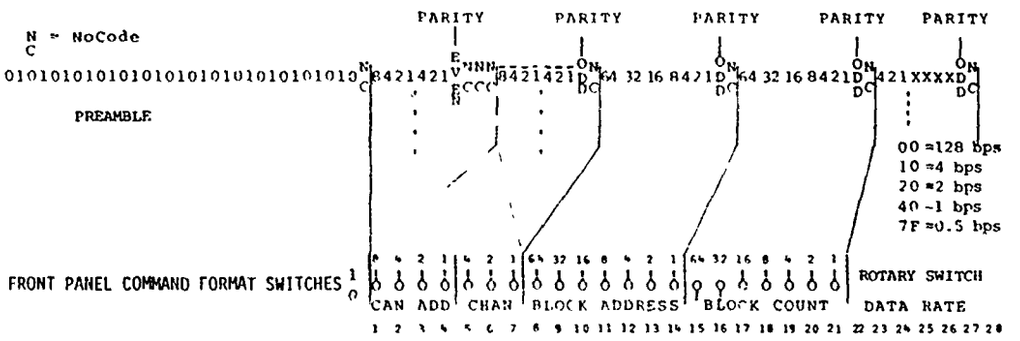
To understand how the proper power supplies are turned on by the Command Receiver Decoder boards (A and B), it is first necessary to become familiar with the code that is transmitted to it. Refer to Table 2 2-1. The code starts with a preamble; the preamble begins with a 010101 and repeats this sequence for 31 bits, ending in a 0. At the end of the preamble, a no-code is transmitted. After the no-code, 8 bits of information are transmitted. The first 4 bits are the canister address. The next 3 bits are the channel address. The 8th bit is a parity bit; this is an even parity and is followed by 3 no-codes. This first word is the only word that is transmitted with even parity. The next 7 bits are the canister address and channel address complemented. The parity bit (Bit 8) is odd parity. This word is also followed by a no-code. The next 7 bits are the block address followed by a parity bit with the no-code separator. The next 8 bits are 7 bits of block count and an odd parity bit followed by a no-code. The last block data is the data rate block. It is also an odd parity block. After this, the receiver will be receiving no-code or noise.

The receiver decoder works by detecting the presence of the preamble which is serially input at U2A Pin 7 of the Command Receiver Decoder Board A. When the decoder receives the first no-code following the preamble, it verifies that the preamble is in proper sequence by U4 Pin 20 prematch of board A, counts the bits as they come in and checks parity. Upon receipt of the next no-code bit, the receiver decoder transfers the canister address and the channel address to the latches.

If the canister is the canister addressed (selected output of U4 to U1B Pin 6 of Board A), the data is latched in permanently. If it is not the proper canister, the data is dropped. When the canister has been selected, the three bits of the channel address U1A, Pins 5,7 and 9 of Board A, are sent to the power supply to bring up the proper channel. The MPU will then come one and test to see if I/O 7 is low and signal the receiver decoder that it is on (by I/O 1, 2, and 3)(while the receiver decoder is receiving the next 8 bits of data and checking the parity), and then take the next data for comparison. It will repeat this process for the remaining blocks of code. The memory (lines of I/O 1, 2, and 3) will then be decoded by U8A of Board B to turn on the transmitter and U8B is used to decode whether the microprocessor should be transmitting a mark or space out through U8B, Pin 6, to the transmitter.

TABLE 2.2-1

CODE



2.2.3 Circuit Descriptions

2.2.3.1 Input Board - 105895

In each memory channel is a multiplex-input board, Figure 2.2-9, which is used to buffer, multiplex, and digitize the signals from two experiment electronic channels or gauges.

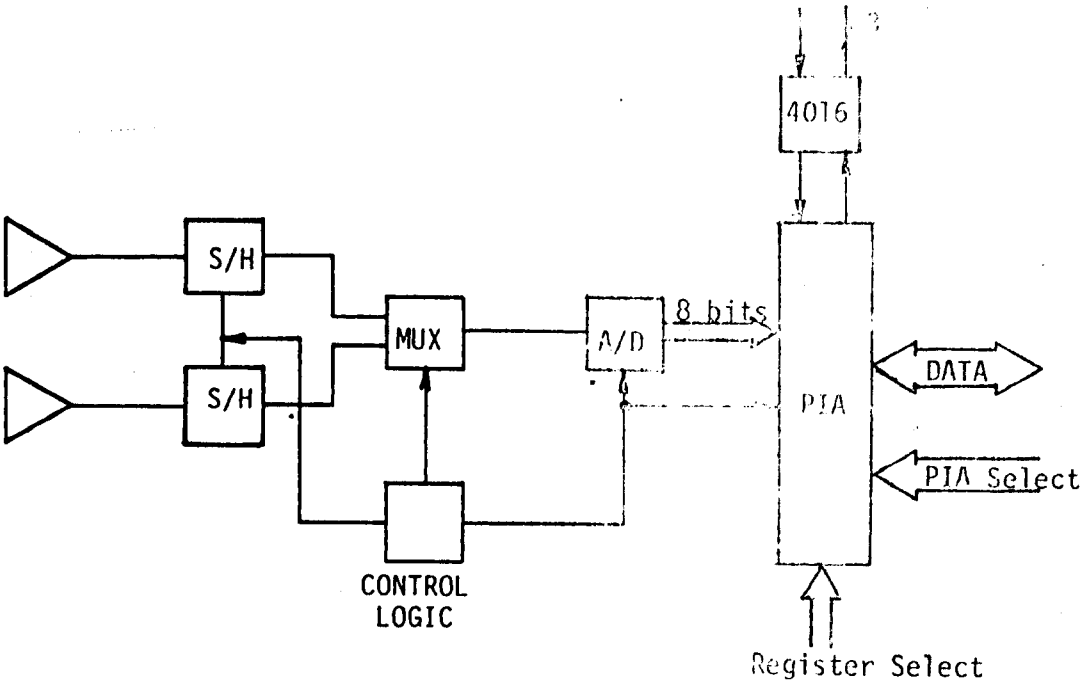


FIGURE 2.2-9
INPUT BOARD BLOCK DIAGRAM

The Input Board consists of two differential amplifiers of unity gain with a roll-off at approximately 15 kHz, two sample and hold (S/H) amplifiers (which hold the data during A/D conversion), a 2 x 1 multiplexer to steer the two S/H outputs to a 10-bit A/D, and a PIA MC6820. The PIA takes the digitized data and provides the proper commands for the A/D, steering of the multiplexer through control logic U8 and U4 during acquisition of data and provides the proper I/O lines for the command receiver decoder during transmission of data, all via the MPU Board.

Referring to the schematic of Figure 2.2-10, the differential input for each channel is provided by a Raytheon 1556 high performance operational amplifier. Common mode rejection is greater than 30 dB, determined mainly by the assumed differences in components between the gauge and the amplifier. The input represents an active load but both the common mode and differential input impedances are greater than 25 kilohms for all conditions. Maximum input voltage must be limited to less than ±15 V single ended or common mode and ±30 V differential. However, the full scale input voltage is ±10 V as determined by the A/D converter. Gain is set to unity, assuming a very low source impedance (<0.01 Z_{IN}), with a possible error of ±2½% determined by the resistors. Note that for future applications, the input resistor could be changed to 5.1 kΩ and that gain could be externally set from 1 to 10 by the appropriate choice of external series resistors.

Each channel has an individual Harris 2425 sample and hold circuit consisting of an input operational amplifier (set for unity gain) in series with a low leakage analog switch and MOSFET unity gain amplifier. An external holding capacitor is connected to the switch output which either tracks or holds the signal when the switch is closed or open, respectively. Although the amplifier 3-dB bandwidth is on the order of 20 kHz, the value of holding capacitance used causes the sample and hold circuit bandwidth to be limited (by the resulting slew rate) to about 16 kHz. However, this is sufficient to insure the input circuits are relatively flat to the design goal of 10 kHz. Note that A/D conversion accuracy is principally determined by the sample hold aperture time which is about 50 to 100 ns in this case. Since the digital resolution is 19.6 mV The slew rate must be limited to less than 0.2 V/μs for 8-bit accuracy, 0.4 V/μs for 7-bit accuracy, etc.

An Analog Devices 7513 semiconductor switch is used to alternately couple each channel to the A/D converter in response to read commands from the MPU. Note that Channel A is always sampled first. The Beckman 876-B10-D1 A/D converter is an 11-bit (10 bits plus sign) bipolar successive approximation device. An alternate circuit version was also designed using the 10-bit Burr-Brown converter as a backup. Although the Burr-Brown was not used on this program, it is recommended in future applications

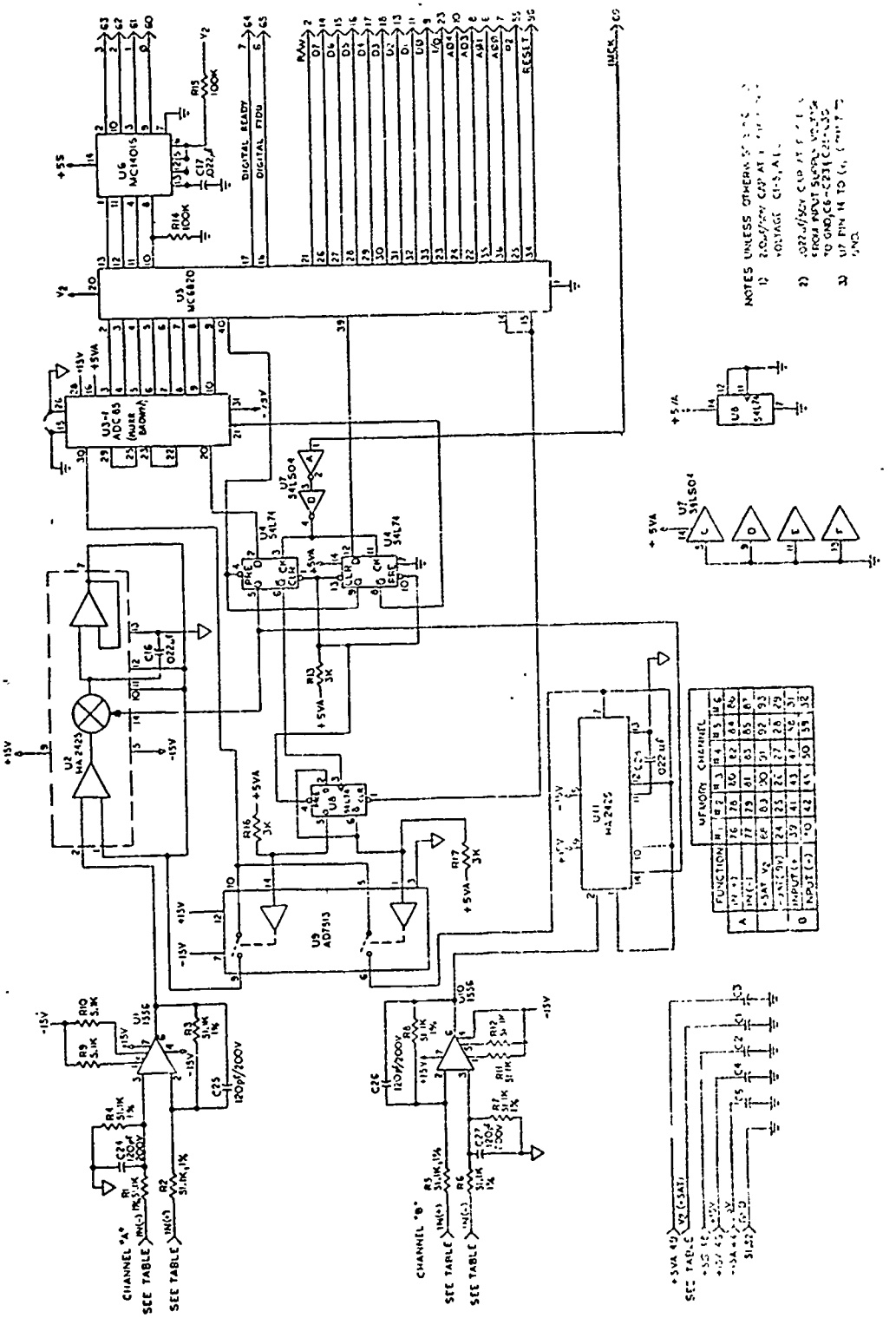


FIGURE 2.2-10A

SCHEMATIC, INPUT BOARD, 105895, Sheet 1

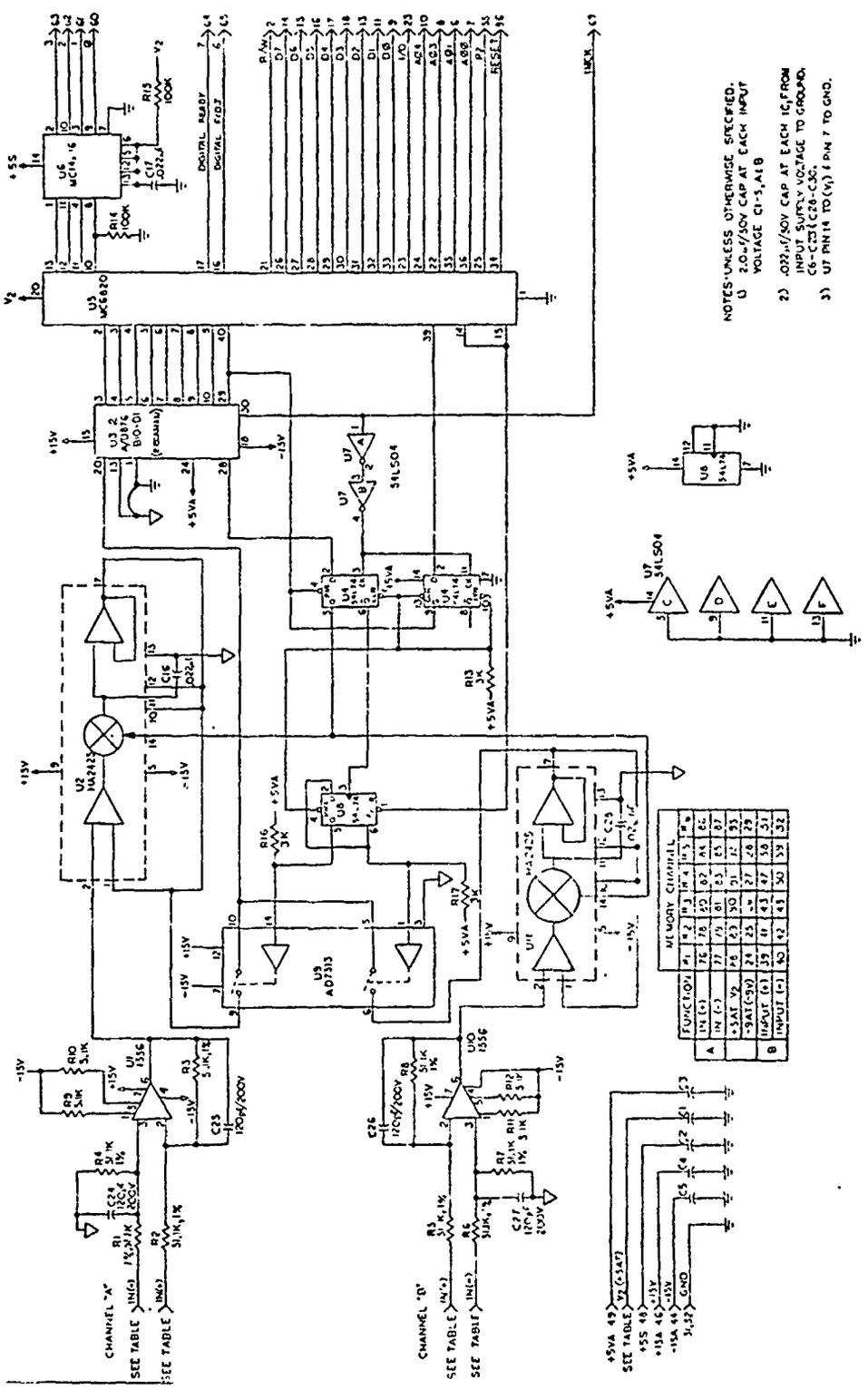


FIGURE 2.2-10B

SCHEMATIC, INPUT BOARD, 105895, Sheet 2

because of its lower cost, lower power consumption, and better performance; e.g., 6 microseconds conversion.

The Beckman output has been truncated to 8 bits (because of the MPU requirements) which achieves 0.0196 V resolution and results in four 5-volt branches of stored data between ±10 volts as shown in Figure 2.2-11.

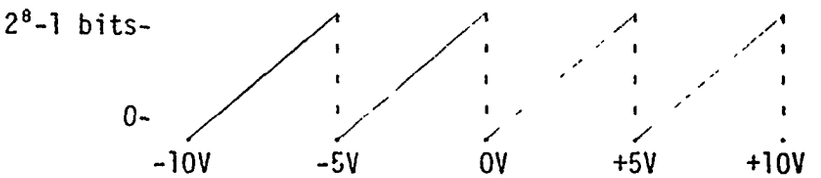


FIGURE 2.2-11

To avoid ambiguity in data, there should be at least two data samples per branch if the signal exceeds 5 volts peak to peak. Each conversion takes 12 microseconds which is faster than required in this system because maximum interchannel switching is limited to 26 microseconds due to the MPU and PROM.

The Motorola MC6820 PIA is wired so that the A inputs are connected to the A/D converter and the B inputs monitor the I/O lines. The 4016 gate is used to connect four of the I/O lines to the MPU so that MPU's that are not brought up will not be connected to these four I/O lines. The A inputs (Pins 2-9) are all programmed as inputs. The B inputs are programmed as follows: Line 0 (Pin 10) is programmed as an input; Lines 1, 2, 3, 4, and 5 (Pins 11-15) are programmed as outputs; Lines 6 and 7 (Pins 16 and 17) are programmed as inputs. CA2 (Pin 39) is programmed as an output. During initialization, Lines 4 and 5 (Pins 14 and 15) are programmed low, clearing U8 which causes the multiplexer to select Channel A. At some later time, these lines are programmed to go high and stay high. CA2 is programmed to go low on every read of the A side of the PIA. When this line goes low, the 1-MHz clock will strobe this transition into the D latch (U4, Pin 12). The low output of the D latch (U4, Pin 9) starts the A/D converter. It is also wired to the interrupt input of the PIA (Pin 40 - CA1), resetting the CA2 output high.

The low signal coming out of Pin 9 of U4 sets the output of the other latch, stopping the sample and hold of both U2 and U11 and putting it in the hold mode. As soon as the converter completes its conversions, U3 Pin 28 goes low and the latch (U4) is reclocked; causing the sample and hold to go back into the tracking mode and changing the state of U4 which selects Channel B input. CA2 then goes low, starting the A/D cycle, sampling Channel B.

2.2.3.2 RAM Board - 105441

The RAM board consists of 8 Intersil 1024x1 CMOS RAM's (IM6508). The 8 RAM's combined are used as a 1024x8 memory with only one R/W line and one CS line, 10 address lines and 8 data lines. See Figure 2.2-12. Therefore, a byte is defined as 8 bits. The 8 data lines are clamped to ground by 8 germanium diodes to prevent these lines from going excessively negative. The input to the RAM and the output to the RAM have been tied together. Using the read/write control, it can be determined whether the RAM will read data or write data. The RAM's are used to store data (write) during acquisition and read out data during transmission. Power is always applied to this board.

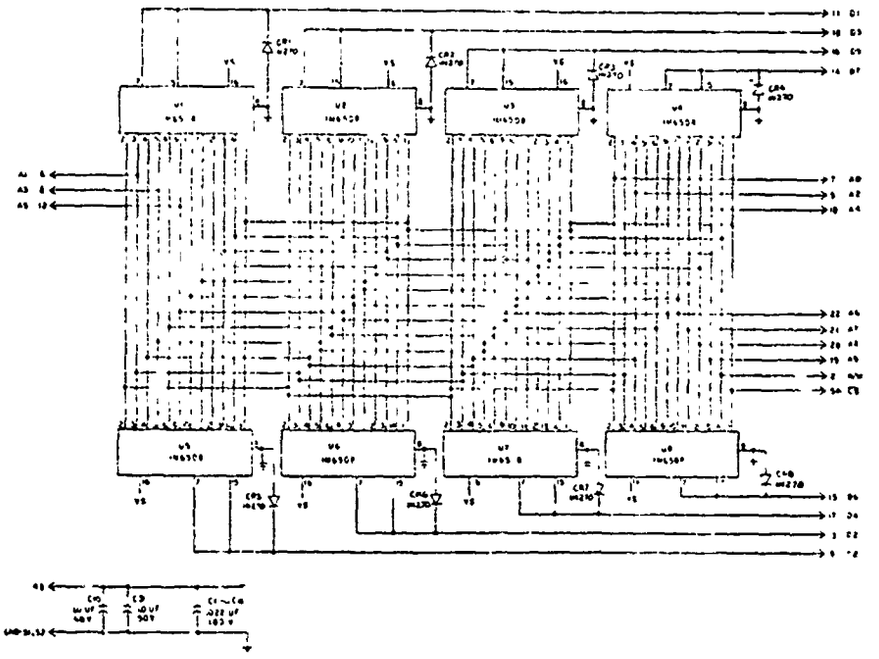


FIGURE 2.2-12

SCHEMATIC, RAM BOARD, 105441

2.2.3.3 MPU Board - 105429

The MPU board supplies the memory system with two PROM's, the MC6800 microprocessing unit, the timing circuitry for the 2-phase clock required by the MPU, the chip select (CS) and the Read/Write (R/W) commands for the RAM board (see Figure 2.2-13).

Refer to the schematic (Figure 2.2-14) for the clock generating circuits to the MPU. The clock is brought in on Pin 68 and divided by 2, generating the 1-MHz clock for the Input board, Pin 69. The clock is again divided by 2 (U8), generating a clock for the MPU. The output of the flip-flop (U8, Pin 5) is put into an RS latch (U7) to generate the two phase of the clock that are not overlapping. The end of ø2 is delayed by two CMOS (Complementary MOS) gates (U9) to give time for the memory to latch in the data. The upper address lines out of the MPU (U1) are decoded by the two sections of the 54139 (U5). Address lines 12 and 13 are used to select whether the MPU is accessing RAM memory, the PROM memory or the Input board (see Table 2.2-2). The highest address is the PROM memory.

TABLE 2.2-2

U5(2) DECODER FUNCTION

INPUTS			OUTPUTS			DEVICE
ENABLE	SELECT					SELECTED
$\overline{2G}$ ($\overline{U17A}$)	2B (A13)	2A (A12)	$2Y_0$	$2Y_1$	$2Y_3$	
H	X	X	H	H	H	None
L	L	L	L	H	H	Input Bd (PIA)
L	L	H	H	L	H	RAM Bd
L	H	L	H	H	H	None
L	H	H	H	H	L	PROM's

If the PROM memory is selected, it is further decoded by the other half of the 54139 using address lines A8 and A9 into one of the two PROM's (U2 and U3). See Table 2.2-3. The additional lower order address bits are fed directly to the PROM's. The address instruction is read

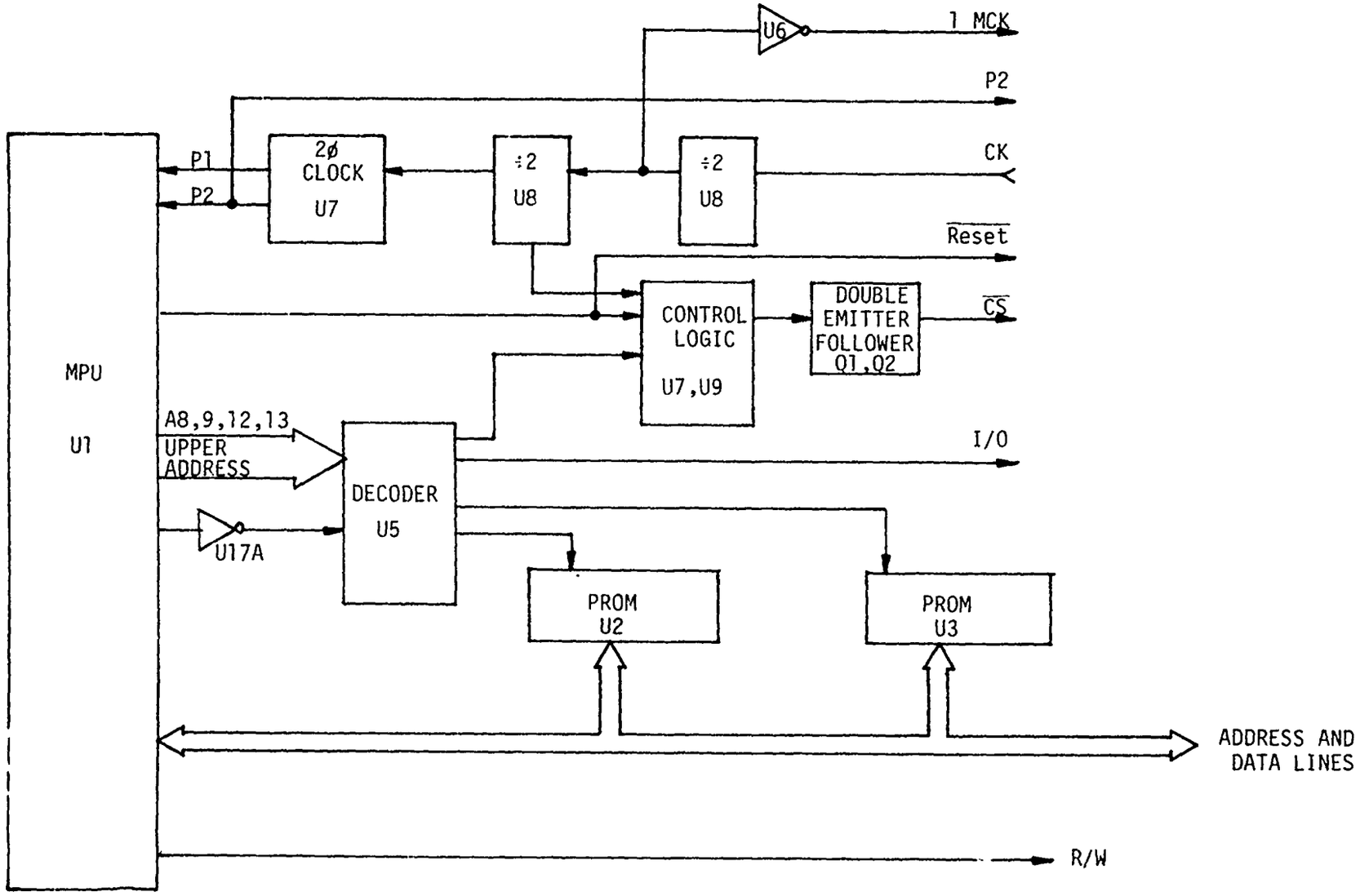


FIGURE 2.2-13

MPU BOARD BLOCK DIAGRAM

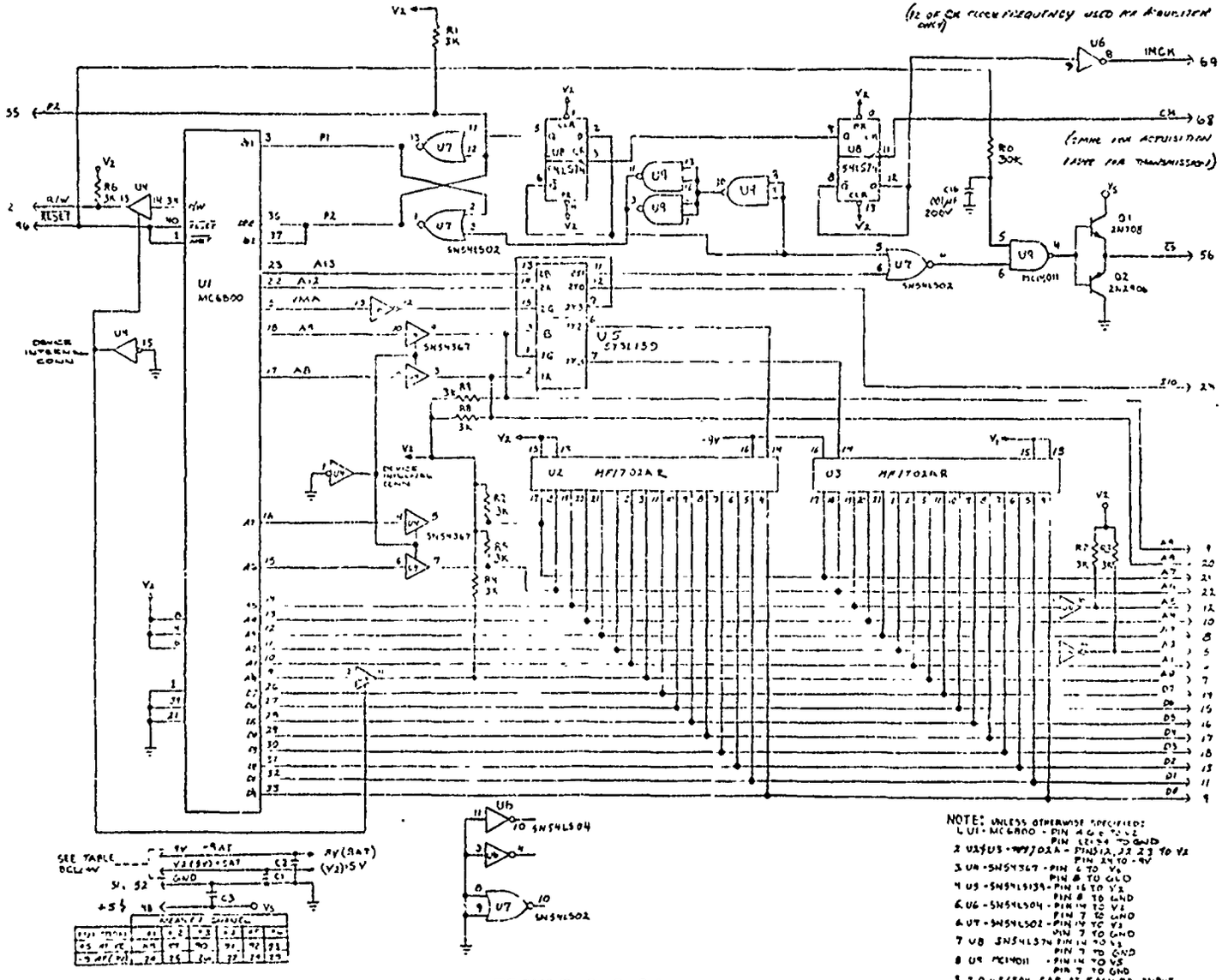


FIGURE 2.2-14

SCHEMATIC, MPU, 105429

TABLE 2.2-3

U5(1) DECODER FUNCTION

INPUTS			OUTPUTS		PROM SELECTED
ENABLE	SELECT				
$\overline{1G}$	$\overline{1B}$ (A9)	$\overline{1A}$ (A8)	$\overline{1Y_2}$	$\overline{1Y_3}$	
H	X	X	H	H	None
L	L	L	H	H	None
L	L	H	H	H	None
L	H	L	L	H	U2
L	H	H	H	L	U3

out of the PROM's and taken into the MPU (U1) which executes the instruction. If the instruction is a reference to the RAM memory, the chip select signal is generated by U7 output Pin 4 and Pin 9. The signal is then buffered by a double emitter-follower (Q1 and Q2). The use of a CMOS gate U9 (which is powered by U5) for the chip select guarantees the chip select line will remain high when the power is turned off, and, therefore, not select the RAM. The delay network made up of R10 and C16 prevents the MPU from disturbing the data and RAM memories when power is first turned on and before the MPU has stabilized.

2.2.3.4 Control and Timing Board - 105405

The Control and Timing Board supplies the system with the clock (Pin 68) and the reset (Pin 96) for the data acquiral channels and a 61-hertz signal (Pin 40) which is used by the receiver decoder. It also generates a Power On command to the power supply (Pin 37), and a signal which indicates to the memory unit that the FIDU signal has been received (Pin 65). There is a constant current output to turn on the experimenter's packages (Pin 38). The inputs to this board are Ready (Pin 74) and FIDU (Pin 75) signals from the EMP protection section, and a signal from the power supplies indicating that they are on (Power Status - Pin 45). Refer to the block diagram in Figure 2.2-15.

The circuits which control the clock output and the reset are shown on the bottom half of the schematic (see Figure 2.2-16). They receive the signal from the power supply, designated Power Status (Pin 45). This circuit (U7) guarantees that after the power supply comes on, the clock will be in operation for at least 64 cycles before the Reset signal goes high, allowing the memory section to function; this is to set up circuits in the memory sections for proper operation. The section starts with a 2-MHz oscillator (U10), which should be set to 2 MHz ±0.1%. The adjustment of this frequency is made by paralleling C1. The output of the oscillator can be checked at U10, Pin 12. U9 is used to gate out the clock. Signals from the upper half of the schematic select 1 MHz or 2 MHz by U9A, Pin 2 high and U9D, Pin 9 low to select 2 MHz and opposite polarities to select 1 MHz. Wnen the power supply has been turned on, the rising edge of the output on Pin 4 of U11 clocks the "1" level of the Power Status line into U7A. The next rising edge of this output (U11, Pin 4) will clock the output of U7A, Pin 1 into U7B, Pin 9 which will cause Reset to go high at Pin 96. U7A, Pin 1 also gates the clock output into the buffers (U2) which drive the memory section (Pin 68). The output of U11, Pin 3 is a 61 hertz signal and the output on Pin 4 is approximately 15.6 kHz. When the Power Status signal goes low, it will immediately reset both parts of U7; this stops the clock and Reset goes low immediately, thus stopping the memory section. The 61 hertz is used to control two timer chains in the upper half of the schematic.

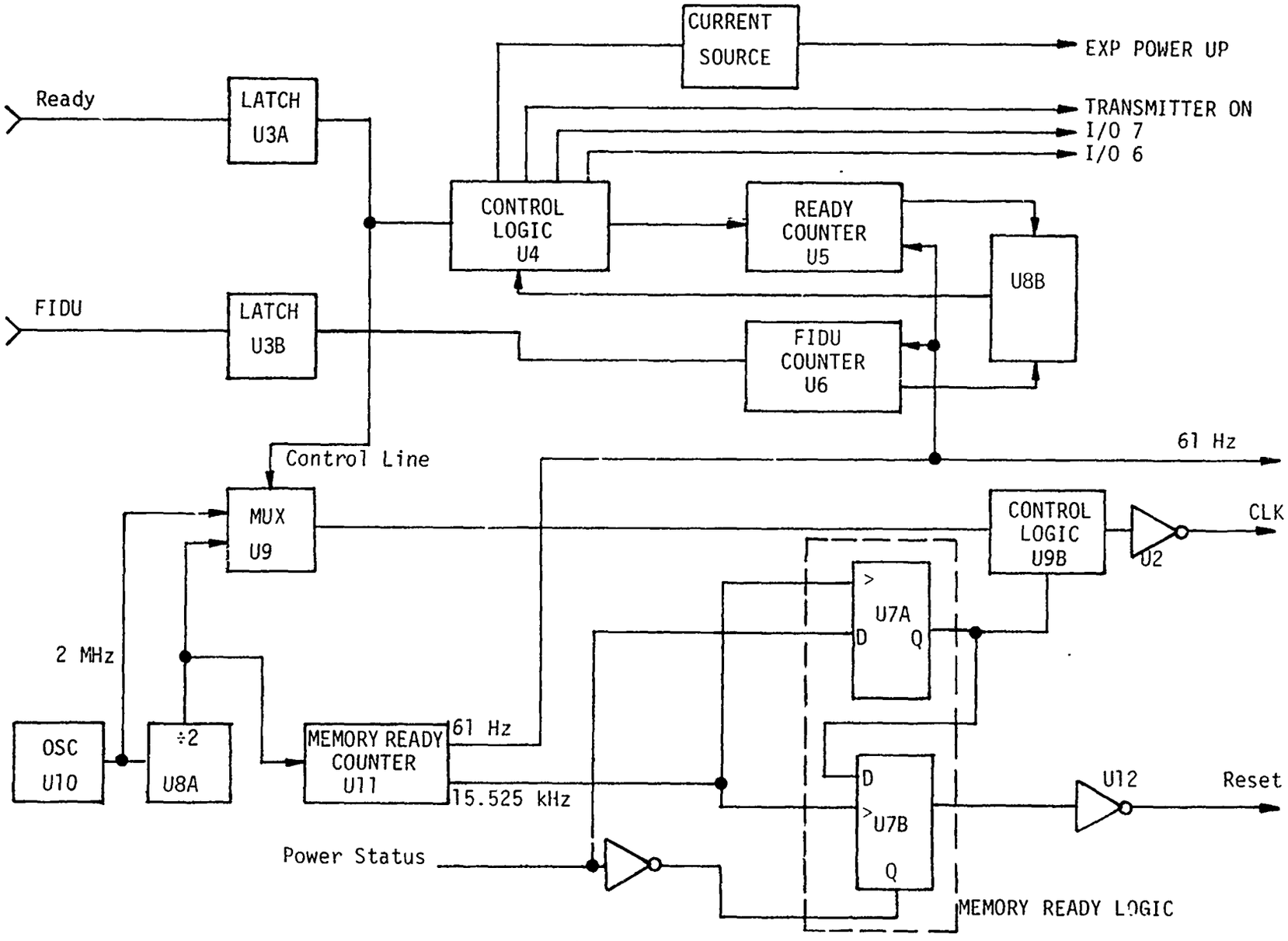
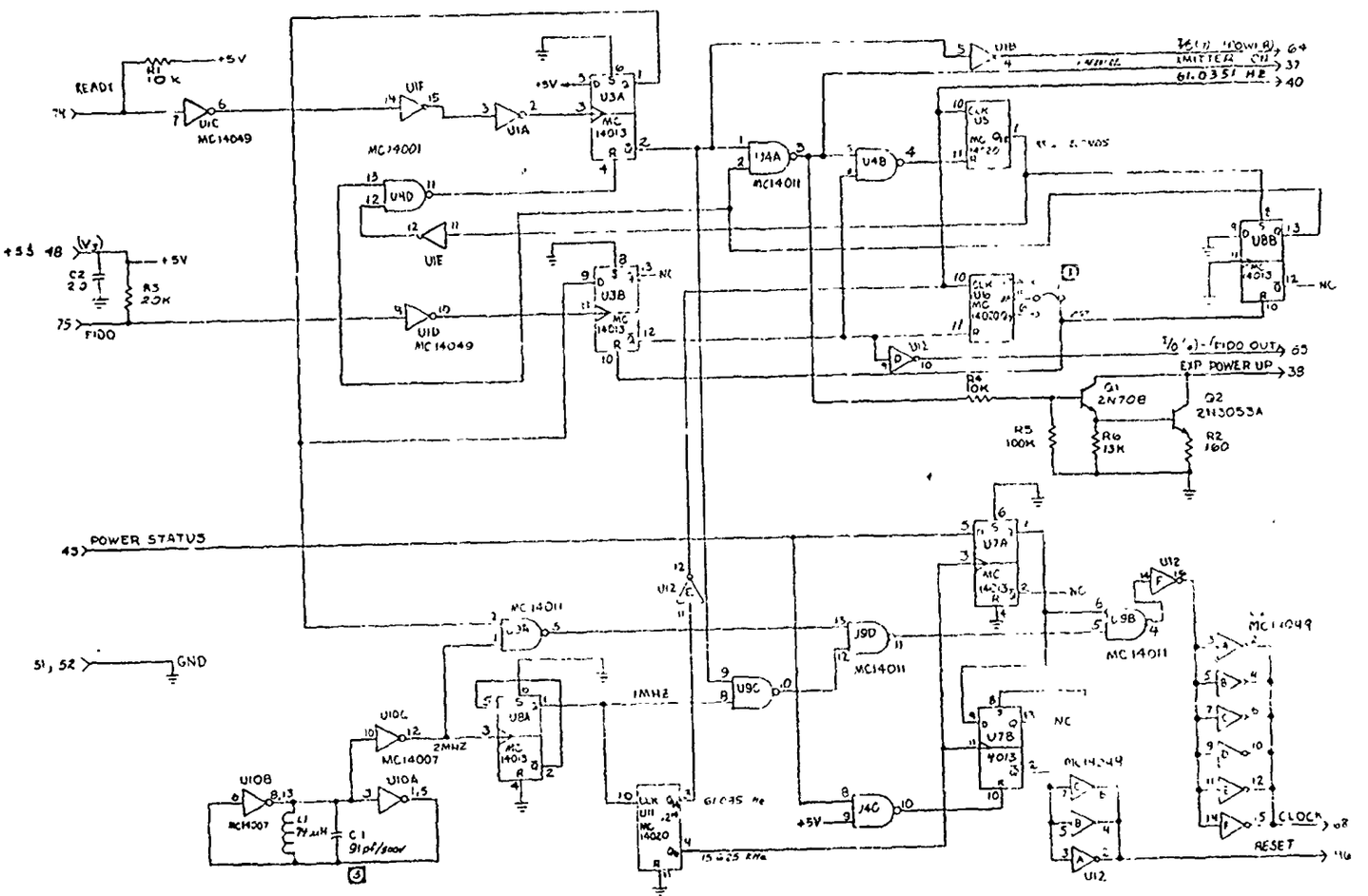


FIGURE 2.2-15

CONTROL AND TIMING BLOCK DIAGRAM



REF	DEVICE	+5V	GND
U1,U1,U1	MC14049	1	8
U3,U3,U3	MC14013	14	7
U4,U9	MC1401	14	7
U5,U6,U11	MC14020	16	8
U10	MC14007	2,11,14	4,7,9

NOTE: UNLESS OTHERWISE SPECIFIED:
1. 10 MF/50V CAP AT EACH 5V INPUT VOLTAGE C2
2. .022 MF/50V CAP AT EACH I C VOLTAGE INPUT C1-1M

FIGURE 2.2-16

SCHEMATIC, CONTROL AND TIMING BOARD, 105405

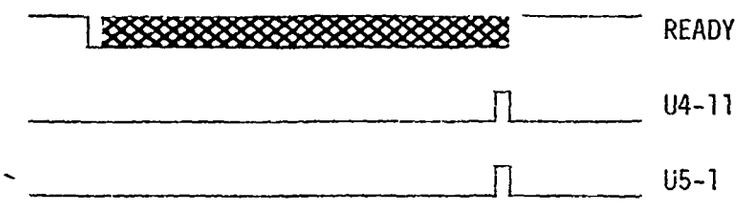
A Ready signal and a FIDU signal are required to enable the acquisition mode. The following is a discussion of how these two signals are handled. When the Ready signal is received, a latch (U3A) is set, turning on the power supplies (Pins 37 and 38), and a counter (U5) is gated on via U4. When this counter reaches its maximum count, it will reset the latch and turn off the power supplies. If, before this counter reaches its maximum count, a FIDU has been received, then a FIDU output will be indicated and it will start its counter. When the FIDU signal is received, the counter (U5), which was counting the Ready signal, will be reset to zero. This Reset condition will be held for as long as the FIDU counter (U6) is running. When the FIDU counter (U6) resets the FIDU latch (U3B), it will also reset the Ready latch (U3A) turning off the power supplies; but at the same time set a new latch, U8B, to keep the Ready counter (U5) running. This Ready counter will then have to time out before the system will receive a new Ready signal. These two counters (U5 and U6), the Ready and the FIDU, count down the 61-Hz signals. The time period for the Ready counter is approximately 30 seconds. The time period for the FIDU counter is approximately one second.

The two transistors (Q1 and Q2) on the board make up a 15 mA constant current source. This source is active as long as the power supplies are turned on and will continue to sink current through the 3-second delay after the end of the FIDU time out.

After a Ready signal has been commanded, a FIDU command must be sent no later than 25 seconds. If a FIDU command is not received within 25 seconds, the system will go back into its standby mode (ready to receive another Ready command).

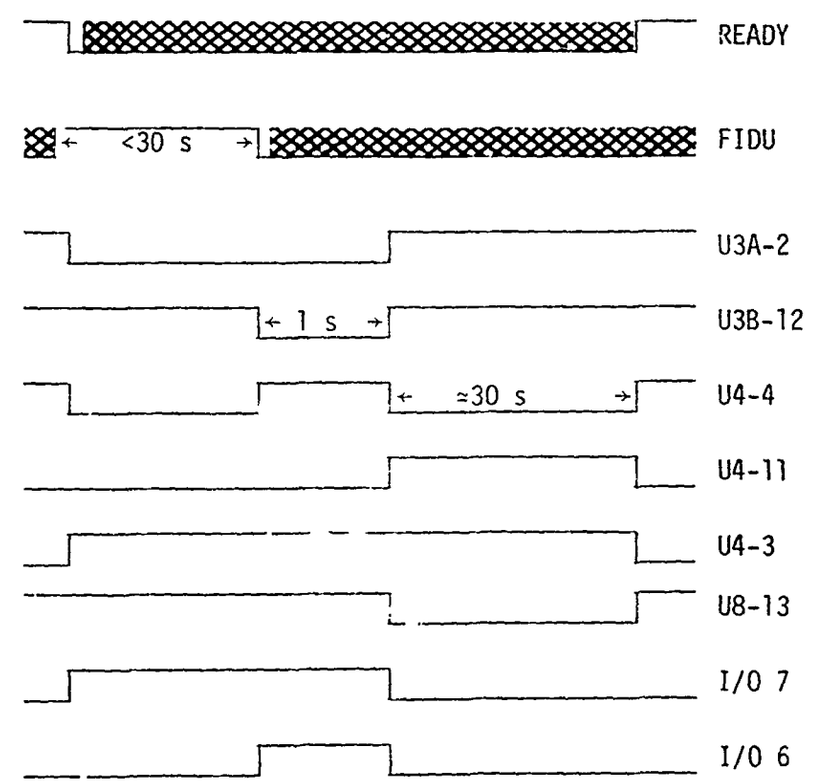
If FIDU has been received prior to 25 seconds after Ready, the acquisition mode has been enabled. Once the acquisition mode has been enabled, it cannot be interrupted or stopped by a signal. Not until 30 seconds after acquisition, when the system reverts to standby, is it possible to initiate an new acquisition.

Reference to the timing diagram below shows what happens if the FIDU signal is not received. When the Ready signal comes in, U3 Pin 2 goes low, allowing U5 to count. U5 Pin 1 goes high, causing U4 Pin 11 to go high, resetting U3 Pin 2, stopping U5 and setting it up ready to receive a new Ready command.



NO FIDU SIGNAL RECEIVED

The second timing diagram below shows the timing that occurs if a FIDU signal is received in the proper time. The Ready signal comes in, setting U3 Pin 2 low. This allows U5 to start counting.



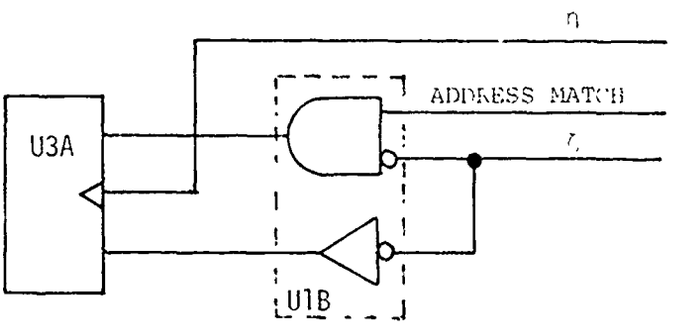
FIDU SIGNAL RECEIVED

The FIDU signal clocks in the high output of U3 Pin 1 into U3 Section B. This causes U3 Pin 12 to go low, allowing U6 to count. At the end of one second, U6 Pin 6 goes high, U4 Pin 11 goes high, U4 Pin 4 goes low and U8 Pin 13 goes low. This causes the I/O 7 output to go low and the I/O 6 output to go low. At this time U5 can again begin counting from zero. When U5 Pin 1 goes high, this terminates the sequence by resetting U8 Section D. When U8D Pin 13 goes high, this sets U4 Pin 11 low, U4 Pin 4 high, and U4 Pin 13 low. Thus the system is again ready to receive a FIDU.

2.2.3.5 Command Receiver Decoder Boards - 105422 and 105423

The function of the receiver decoder is verification of the preamble, checking of the canister address and checking parities. If any of these tests fail at the time of the receipt of a signal, the receiver decoder will turn off the memory channel. A detailed description of the process follows, and a block diagram will be found in Figure 2.2-17. The schematics may be found in Figures 2.2-18 and 2.2-19.

Board A (105422) contains the shift register (U2) which takes the data in from the receiver, a second shift register (U5) to which the data are parallel transferred from the first shift register and clocked out by the memory unit, and a third shift register (U6) which is parallel loaded with housekeeping data at the same time the data is loaded into the second shift register. U2 is the shift register that receives the data from the command receiver. These data are transferred to U5 upon receipt of the no-code (which is discussed later). At that time, housekeeping data are strobed into U6. U4 is the channel canister decoder. If the canister has been selected, the selected output of U4 will go high. U1B has been wired to behave as an AND gate; it will AND the parity data with the canister address match (high output of U4) strobing the canister address into U3A. U1A latches the channel address and presents it to the power supplies. (U1 is a dual 4-bit latch with tristate output that has been used to achieve the equivalent logic diagram shown below.)



The data from one output of U1B (i.e., Pin 17) is made available to the J input of the J-K flip-flop. The parity bit is put on the disable input. Therefore, by having the parity bit proper and the proper address, U3A will be set to the proper level. U1C output of Board B is

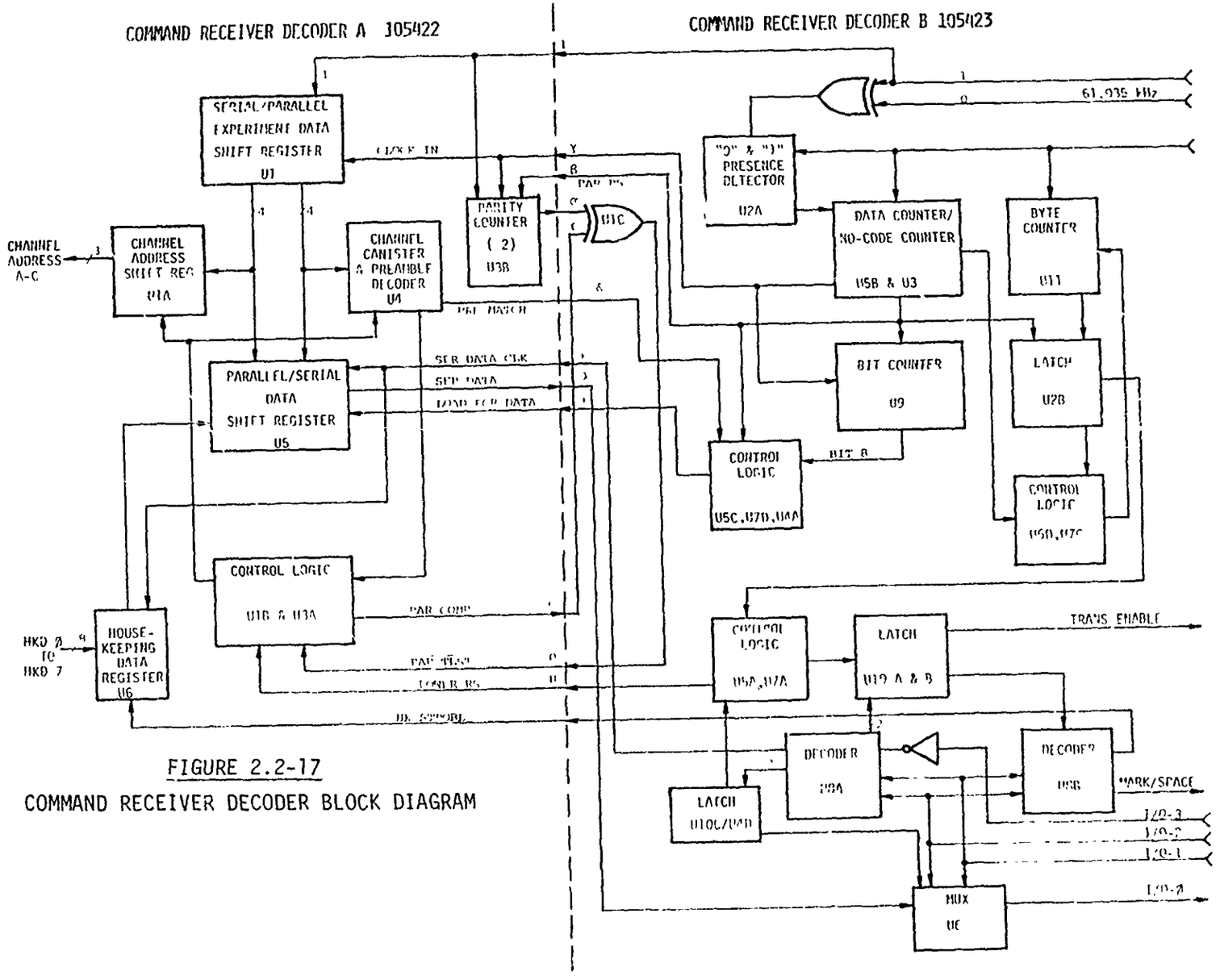
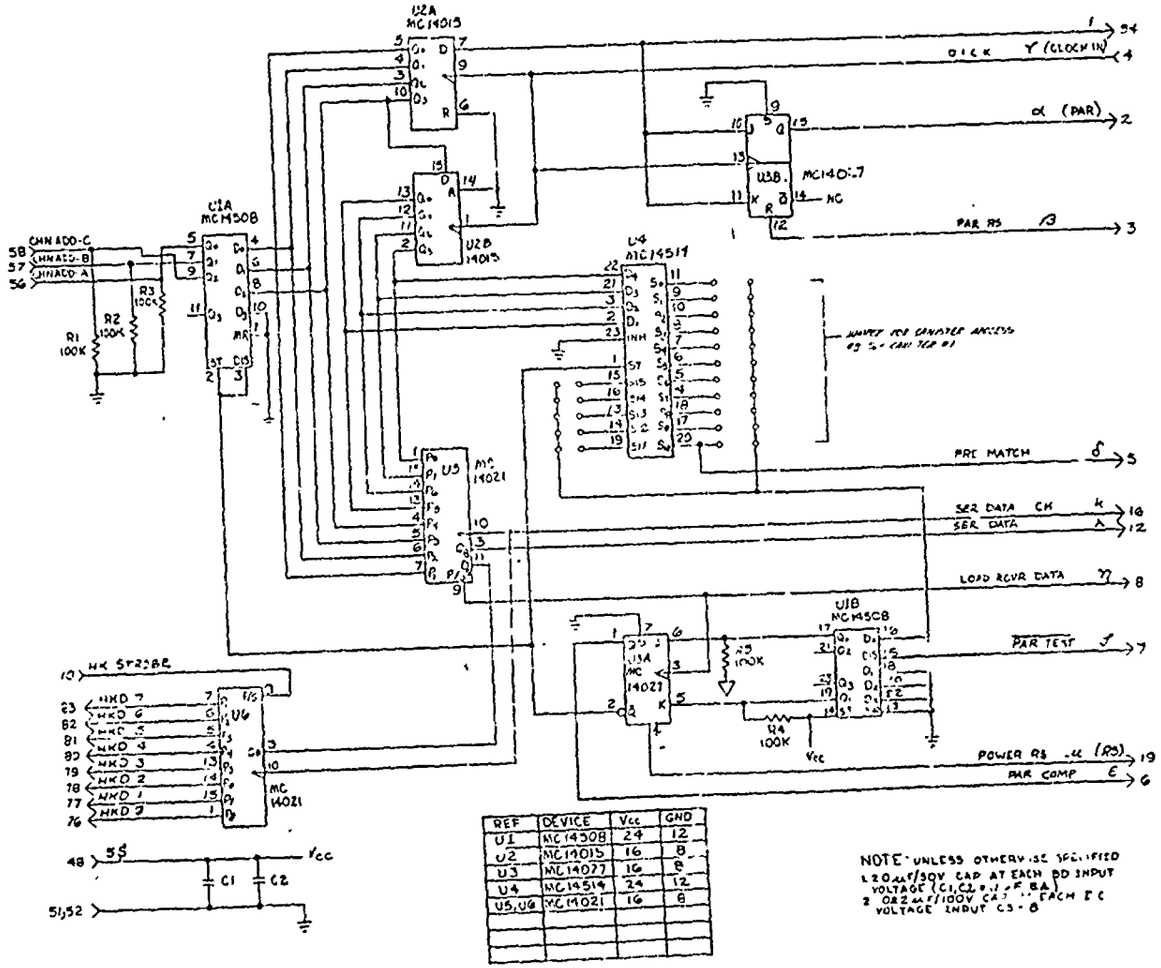


FIGURE 2.2-17

COMMAND RECEIVER DECODER BLOCK DIAGRAM

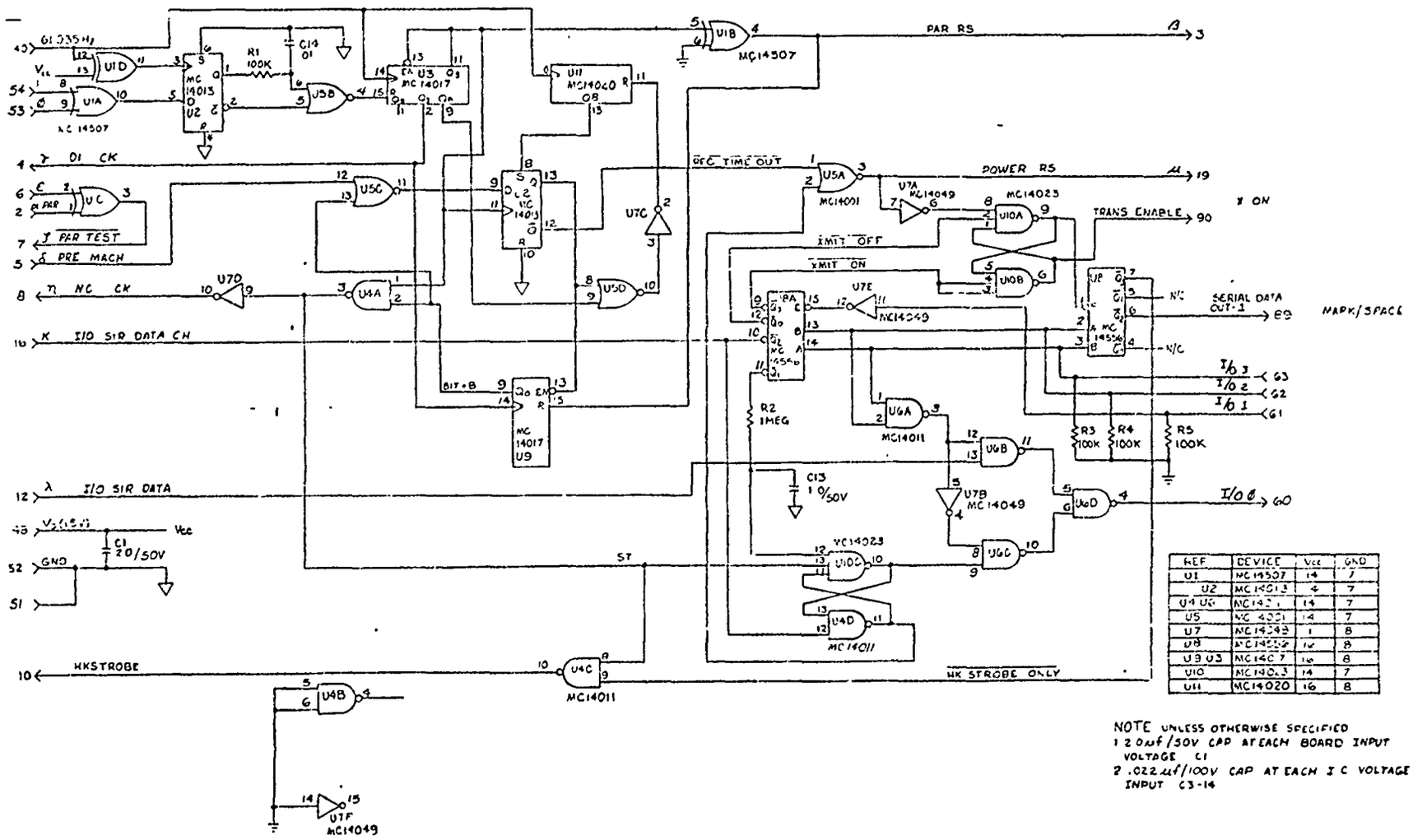


REF	DEVICE	Vcc	GND
U1	MC14508	24	12
U2	MC14015	16	8
U3	MC14077	16	8
U4	MC14514	24	12
U5,U6	MC14021	16	8

NOTE: UNLESS OTHERWISE SPECIFIED
1 20 μF/30V CAP AT EACH DD INPUT VOLTAGE (C1, C2 0.1 μF EA.)
2 .022 μF/100V CAP EACH EC VOLTAGE INPUT C3 - 8

FIGURE 2.2-18

SCHEMATIC, COMMAND RECEIVER DECODER BOARD A, 105422



REF	DEVICE	Vcc	GND
U1	MC14507	14	7
U2	MC14013	4	7
U4 U6	MC14011	14	7
U5	MC 4001	14	7
U7	MC14049	1	8
U8	MC14536	16	8
U9 U3	MC14017	16	8
U10	MC14023	14	7
U11	MC14020	16	8

NOTE UNLESS OTHERWISE SPECIFIED
1 .2 0uf/50V CAP AT EACH BOARD INPUT VOLTAGE C1
2 .022 uf/100V CAP AT EACH I C VOLTAGE INPUT C3-14

FIGURE 2.2-19

SCHEMATIC, COMMAND RECEIVER DECODER BOARD B, 105423

used as an inverter of PAR (α) to provide $\overline{PAR}$ (ζ)for the K input. U3B is a J-K latch which will be toggled every time there is a 1 input from the receiver; thus it will end up counting modulo 2 the number of 1's that have been clocked in. By taking the output and putting it through an Exclusive OR (U1C on Board B), a parity check is made on the bytes of data, where ε is the parity even/odd flag generated from U3A, Board B (105423).

The microprocessor communicates with the receiver decoder by four lines. They are labeled I/O-0, -1, -2, and -3. I/O-1, -2, and -3 are inputs to the receiver decoder. I/O-0 is an output from the receiver decoder to the microprocessor. A 2-line-to-4-line decoder, U8A, is used to decode signals that come in from the microprocessor to either clock the shift register, turn off the MPU when the MPU has completed its transmission, switch over and determine if the receiver has received a block of data, and turn on and off the transmitter (refer to Table 2.2-4). The other half of U8 (U8B) is used to decode, when the transmitter is turned on, and determine whether the microprocessor should be transmitting a mark or space out through the transmitter. U6 is used only to multiplex between the data that are stored in the shift register U5 of Board A and the latch made up of U10C and U4D. U10C is reset every time the microprocessor transmits data from the shift register. It is set every time the unit detects a no-code or it can be set by the microprocessor to turn the whole system off. U11 is a counter which counts a period of time larger than 1 byte time of the receiver. If U11 overflows and the latch, U10B and U4D, has not been reset, the entire system is reset and the power turned off. Since this counter U11 will have already counted out when the MPU wishes to turn off the system, setting the latch (U10B/U4D) will turn the system off.

U2 is used with U1A to detect the presence of a 1 or a 0. When a 1 or a 0 is detected by the Exclusive OR gate (U1A), it clocks U2. The output of U2 is differentiated and used to reset the counter U3. U3 generates an output between 16.4 and 32.8 ms to clock in the data that has been detected. If U3 is not reset by 130 to 146 ms, it detects

the fact that a no-code has come through. This no-code transfer is used to test and transfer the data (U5) on Board A, clearing the parity latch (U3B of Board A) and the bit counter U9. U11 and half of U2 (the section with Pins 8, 9, 10, 11, 12, and 13) constitute a time which will count for a period a little longer than one byte time. When the preamble is being received, prematch will detect the correct preamble. At the first no-code that occurs at the end of the preamble, the latch U2 will be reset. This will cause U11 to start counting. The next time a no-code is received, the fact that U2 is already reset allowing U9 to count to 8 will cause U2 to remain reset and will reset the counter U11. It will continue to repeat this process through each no-code until all the data have been received. At that point, the unit will stop receiving no-codes and good data and U11 will time out.

U9 is reset on every no-code that is received. It will be clocked every time the data are transferred into the shift register (U2 of Board A) from the receiver. If U9 has reached the count of 8 at the time the no-code is detected, it will cause the data to be transferred over to the shift register (U5 of Board A) for the microprocessor to take. If, for some reason, it fails to meet this count, the data will not be transferred.

TABLE 2.2-4

U8A FUNCTIONS

E	B	A	Q_0	Q_1	Q_2	Q_3	
0	0	0	0	1	1	1	TRANSMITTER OFF
0	0	1	1	0	1	1	TURN OF MPU
0	1	0	1	1	0	1	CLOCK SHIFT REGISTER
0	1	1	1	1	1	0	DETERMINE IF RECEIVER HAS RECEIVED BLOCK OF DATA
1	0	0	1	1	1	1	N/A

Table 2.2-5 shows how commands from the microprocessor to the receiver decoder are decoded. The column labeled TRAN determines when the system is in the Receive or Transmit mode. 3,2,1 refers to the I/O bits and NOP means no op. All zeros constitutes a no op. When Bit 1

TABLE 2.2-5

TRAN	TO RECEIVER I/O-3	I/O-2	I/O-1	OPERATION	On I/O-0
0	0	0	0	NOP	DATA (0)
0	0	0	1	TRAN←0	DATA (0)
0	0	1	0	NOP	DATA (0)
0	0	1	1	DATA N← DATA N+1	DATA (0)
0	1	0	0	NOP	DATA (0)
0	1	0	1	Power←0	DATA (0)
0	1	1	0	NOP	Flag
0	1	1	1	TRAN←1	Flag
1	0	0	0	X_{OUT}←1	DATA (0)
1	0	0	1	X_{OUT}←1; TRAN←0	DATA (0)
1	0	1	0	X_{OUT}←1	DATA (0)
1	0	1	1	X_{OUT}←1; DATA N← DATA N+1	DATA (0)
1	1	0	0	X_{OUT}←0	DATA (0)
1	1	0	1	X_{OUT}←0; Power←0	DATA (0)
1	1	1	0	X_{OUT}←1; DATA 8-15 HK 0-7	Flag
1	1	1	1	X_{OUT}←1; TRAN←1; DATA 8-15← HK 0-7	Flag

/Flag/Data Ready ← 1

← means "is replaced by". For example, take the next-to-last line; X_{out} is replaced by 1, TRAN is replaced by 1 (i.e., transmitter is turned on), data bits 8 through 15 are replaced by housekeeping data bits 0 to 7, and at the same time the microprocessor is looking at the flag bit. Or, take the fifth line from the bottom; X_{out} is replaced by 1 (i.e., transmitter is transmitting a mark), and data bit N is replaced by data bit N+1.

is 1, the transmitter will be turned off. It can be seen that if all three I/O lines become 1, then the transmitter will be turned on. When I/O-2 is 1 and I/O-1 is 1, data will be shifted and the microprocessor will look at the next bit of data. The last column shows what appears on I/O-0; i.e., note flag is available for inspection when I/O-2 and I/O-3 are both 1. The flag can be inspected without turning on the transmitter by leaving I/O-1 in the 0 state. When transmitter is on, housekeeping data can be loaded; or brought to the MPU for use.

2.2.4 Software Program Description

The DNA Underground Telemetry System Program is divided into two subprograms. One subprogram acquires and stores the data in a read and write memory and begins at the label AQUIRE. The second subprogram controls the transmission of stored data and is labeled OUTD. There is a short initial portion of the program which sets up the peripheral interface adaptor (PIA) and provides for the selection of one of the two subprograms. Refer to the flow diagram of Figure 2.2-20. At the end of the fixed program code there is a "blank" (zeros) area in which variables are stored for control of individual canisters and channels. The setup of this table is discussed in the end of this subsection.

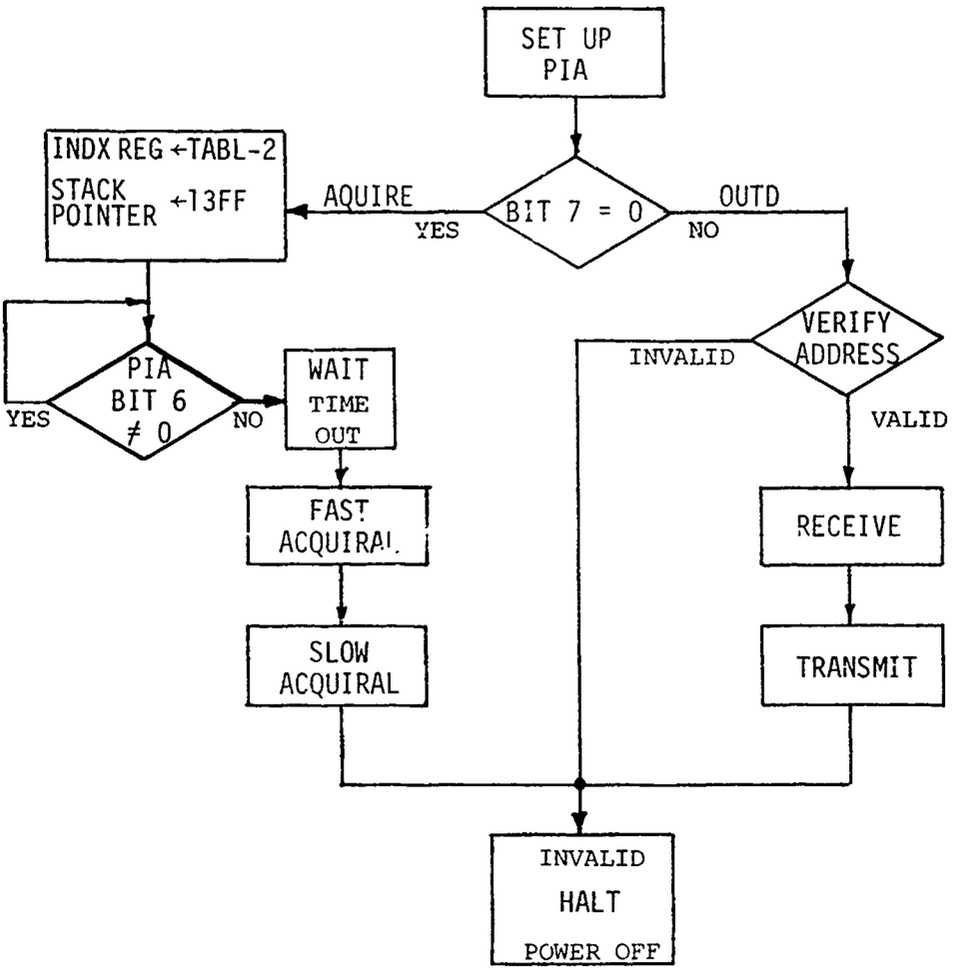


FIGURE 2.2-20
PROGRAM FLOW DIAGRAM

2.2.4.1 Setup and Subprogram Selection

The PIA is set up at the start of the program. Peripheral interface register A (PIRA) is set to serve as input from the analog-to-digital converter. Register B (PIRB) communicates with the receiver and transmitter. Lines 1 through 4 are set as outputs from the B register, the remaining lines are inputs.

Data is examined by the microprocessor from PIRB. If the most significant bit is zero, transfer is made to the data transmission subprogram (OUTD). Otherwise, the procedure for acquiring and storing data (AQUIRE) is entered.

2.2.4.2 Data Acquiral and Storage

Stack and index pointers are initialized in the instructions from label AQUIRE to ED. In the loop ED, the microprocessor awaits a signal on line 6 of the PIRB. When this flag bit is found, the program enters a waiting loop WAITO; the waiting time is determined by the number loaded into the index register from (TABL-2,TABL-1)=TIMOUT. One cycle around the loop takes 26 microseconds, so that the waiting time may be selected to be an integral number of that period. Data from the A/D converter is then sampled and stored. The sample rates - except for the first two groups - and the number of samples in each group are stored in a table labeled TABL. The number of samples in each group may be selected to be between 1 and 255. The first group, labeled GROU1, has a fixed sample time of 26 microseconds; the second, GROU2, has a fixed time of 52 microseconds. Subsequent group sampling rates may be varied. The sample rate in microseconds is determined as $26 \times N + 78$, where N is the relevant number stored in the table. This variable-time loop begins at label GROPK, reading two numbers from the table at a time; the number of samples and the value N defined above. If, however, the value for the sample number is zero, the program ends with a transfer to INVLD which sends a Power Off signal on the three peripheral interface register lines designated as outputs. Refer to the flow diagram in Figure 2.2-21.

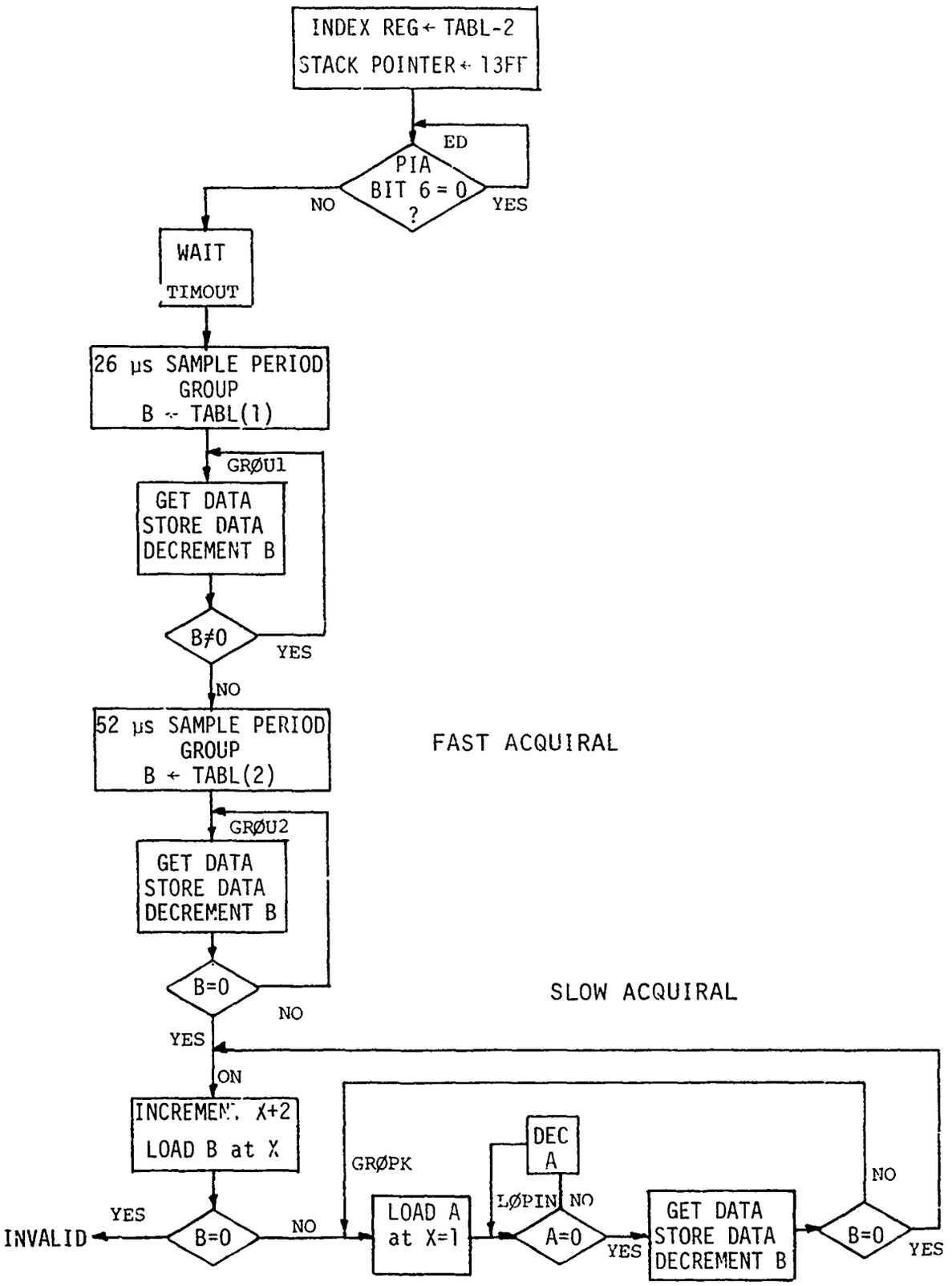


FIGURE 2.2-21

FLOW DIAGRAM - AQUIRE

2.2.4.3 Data Transmission

If, at label POWER, Bit 7 of interface register B is not set, transfer is made to the subprogram which controls data transmission (OUTD).

Transmission Control by Data from the Receiver - Initially, subroutine LOOKFL is called to look for a flag on Line 0 of interface register B. If the flag is not found within a few seconds, power is turned off at INVLD. Otherwise, the serial data received on peripheral register B Line 0 is converted to parallel data in accumulator A by the routine labeled SEREA8. As received, each parallel bit is placed in Bit 0 of accumulator A. Previously received bits are stored in location M2. These bits are added to accumulator A, shifted one position to the left, then deposited back in M2 for the next looping. This procedure is done eight times, the count being held in location COUNT.

Within the previously discussed subroutines are references to subroutines MS and DS. These are relatively short and relatively long waiting periods required by the receiver system. Transmissions to address PIRB occurring during these routines are instruction codes for the receiver system on the output lines of peripheral register B. These codes and their function are not discussed here, as they are external to the microprocessor software. For discussion of timing and receiver system codes, refer to documentation on the receiver system.

The first call to subroutine LOOKFL returns the canister channel address to accumulator A. The last bit received is a parity bit, which is removed by a right shift which truncates it. Comparison is made with the address stored in the read only memory. If the comparison is not successful, power is turned off at INVLD. Eight bits of housekeeping data directly follow the canister/channel address. Therefore, the flag is not looked for, but the subroutine converting serial to parallel data is entered at SEREA8 directly. The data are stored at HOUSE1. The second call to LOOKFL proceeds similarly, except that this time comparison is made with the complement of the canister/channel address.

Three subsequent calls to LOOKFL result in the microprocessor receiving and storing the number of the desired starting data block, the number of blocks which are desired to be transmitted, and a code indicating the rate at which the data bits are to be transmitted. These data are stored respectively in locations GROUP, NOBLKS, and RATE. The parity bit in each case is masked by a logical AND instruction, so that the stored number is, in effect, twice the transmitted number. This fact later saves a multiplication by two in a procedure which utilizes the starting group number.

Data Transmission - At label TURNON, the transmitter is turned on by putting ones on all three output lines of peripheral register B (PIRB). Four bytes of preamble are transmitted first, by four transfers to the subroutine PATOSE. The transfer is effected in two steps: To PASTEP and thence to PATOSE. (The preamble serves to synchronize transmitter and surface receiver.)

The subroutine PATOSE converts eight bits of data in accumulator A to a serial data stream. In the loop PTOS, the bits are scanned one by one by storing the data in M2, testing the leftmost bit in accumulator A, shifting and so on. This procedure is followed seven times (= the initial value in COUNT) in the loop PTOS, the last of the eight bits is tested in an ending routine. (In these routines, the subroutine generating a parity is called. Location M, together with B, is used to count modulo 2 the number of bits equal to one.) The result of the bit test is transmission of code to the transmitter on the three output lines of peripheral register B. If the bit is zero, the value of "zero" is sent first, then the value of "one". If the bit is one, the order of transmission is reversed; "one" is sent first, then "zero".

Between each transmission of these codes, the subroutine BTRATE is called. The waiting time of this routine is determined by approximately multiplication of the times of two loops, labeled SET2 and OPS. The constant determining the number of times the inner loop, SET2, is done is stored at the address immediately following the label. The number of times the outer loop is done is determined by the value stored in RATE. Thus, the

period of the routine BTRATE is nearly proportional to the number stored at location RATE. Entry in the routine at DS results in a different constant being used in the outer loop. This permits use of most of the code of the routine DS for a fixed time waiting period. This procedure is called at various points in the program when the system requires a pause.

If the subroutine BITS9 is called, the parity bit is coded and sent following the eight data bits. Note that entry to the routine at label BITS9 results in an indexed loading of the accumulator A. An entry one instruction beyond the label results in transmission of data placed in that accumulator before the call to the subroutine.

The procedure which follows the getting and transmitting by BITS9+2 of HOUSE1 calculates and loads the index register with the starting address of the requested group. If the number stored is $G_{\#}$, the starting address in read-and-write memory is given as

$$A_0 = 13FF - 4G_{\#}$$

Recall that the stored number is twice the number obtained from the receiver. Each group contains eight data items. The subroutine BITS9 is called, loading data from the indexed location in the read-and-write memory and decrementing the index register. As many groups or blocks of eight data items are transmitted as was requested by the number stored in NOBLKS. The loop, labeled GRP, is structured so that if NOBLKS equals 0, no data are transmitted at all. When the requested number of blocks has been sent, the program transfers to the power shutdown procedure INVLD.

2.2.4.4 Preparation of the Table

The table of variable quantities used by the program is in one area of PROM #2. These locations are initially blank so that each #2 PROM may be individually loaded with table data. The loading is to be done with the PRO-LOG Series 90 Programmer. Refer to the instruction manual for this equipment for details on the method of implementing data entry into the desired locations.

The tabulated variables begin in hexadecimal address 3FAE, labeled CANADD. See Table 2.2-6 for a summary of locations and contents. The number of locations needed is determined by the number of pairs of data required to determine the number of samples and sample rates for the variable-rate sampling groups. The last address available in the PROM is 3FFD, providing approximately 77_{10} locations for these data. The purpose of each of the items in the table and the means of determining the value to be inserted are discussed below.

TABLE 2.2-6

ADDRESS	LABEL	ITEM
3FAE	CANADD	Canister and Channel Address
3FAF		Time out (most significant)
3FB0		Time out (least significant)
3FB1	TABL	# of samples in the first group
3FB2		# of samples in the second group
3FB3		# of samples in the third group
3FB4		sampling-rate code (third group)
3FB5		# of samples in the fourth group
3FB6		sampling-rate code (fourth group)
etc.		

Canister and Channel Address - The first item in the table, at the label CANADD, is the canister and channel number which is a two-digit hexadecimal number stored as one byte. The first digit selects the canister and the second digit selects the channel.

Time Out - The next two locations (TABL-2, TABL-1) determine the initial waiting period or "time out" to the start of data sampling. This is a double-precision number which is loaded into the index register. The number is decremented by a loop in the program which takes 26 microseconds. Thus, the time to first sample is given by

$$t = (\text{TIMOUT}) \times 26\ \mu s + 26\ \mu s;\ (\text{TIMOUT}) \neq 0.$$

It is to be noted that the most significant part of the double-precision number is loaded into the lower address location. The largest number that may be placed in TIMOUT is FFFF (hex) which will produce the longest waiting period, 26 microseconds longer than for FFFF.

Data Sampling Groups - There are two types of data sampling channels. The first are fixed sample time groups with variable numbers of samples only. The second type have variable sample rates as well.

A. Fixed-Rate Groups - The sample rate of the first group is 26 microseconds; of the second group the rate is 52 microseconds. The number of samples may be chosen in the range 1 to 256 for each group. The value for the first group is at location TABL. Two-hundred and fifty six is selected by entering 0, the other numbers are entered identically.

B. Variable-Rate Groups - Pairs of data are required for the variable-rate groups (3 and up). The first item is the number of samples, the second determines the sampling rate. In these groups, the entry of a zero in the location for sample numbers results in termination of the program; that is, it signifies the end of data. Then the entry of a number, other than 0, specifies that number of samples in the range 1 to 256.

2.3 EXPERIMENT INTERFACE

Since most of the experiment function details are not known to us, the purpose of this section is to describe the system interface design considerations in general, record the final internally programmed data acquisition parameters and comment on known conditions that may be useful for reference.

The gauges and experiment (gauge conditioning) electronics were constructed by WES and assigned to telemetry system channels as shown in Table 2.3-1.

TABLE 2.3-1
WES GAUGE ASSIGNMENTS

	TELEMETRY CANISTER					
	210'		300'		400'	
CHANNEL	WES #	FUNCTION	WES #	FUNCTION	WES #	FUNCTION
1A	3	Vertical DX	3	Vertical DX	3	Vertical DX
1B	3	Horizont DX	3	Horizont DX	3	Horizont DX
2A	3	Horizont Acc	3	Transverse DX	3	Transverse DX
2B	4	Vertical DX	4	Vertical DX	4	Vertical DX
3A	4	Vertical Acc	4	Horizont DX	4	Horizont DX
3B	4	Horizont Acc	4	Horizont Acc	4	Transverse DX
4A	3	Stress	3	Stress	3	Stress
4B	5	Vertical DX	5	Vertical DX	5	Vertical DX
5A	4	Stress	4	Stress	4	Stress
5B	5	Vertical Acc	5	Horizont DX	5	Horizont DX
6A	5	Stress	5	Stress	5	Stress
6B	5	Horizont Acc	5	Horizont Acc	5	Transverse DX

NOTES: 1. Channels A and B are multiplexed inputs to the same memory. They are alternately sampled at the same rate (see sampling illustration in Section 2.3.4).

2. DX = velocity gauge
Acc = accelerometer gauge
Stress = ytterbium stress gauge (SRI).

All gauges were located roughly 100-300 feet (30-100 meters) from the telemetry system canisters via junction boxes and hardened cables (except the

stress gauge cables were outside the conduit) also constructed and installed by WES. Velocity and accelerometer gauge electronics were located in the gauge canisters. Stress gauge electronics and miscellaneous functions were supplied to Develco for final mechanical assembly and installation in the telemetry canisters. The three principal functions provided by the telemetry system for the experiment electronics (in addition to data digitizing and storage, etc.) were power, experiment on/off commands, and a protected signal input as shown in the block diagram, Figure 2.3-1.

2.3.1 Experiment Signal Input

The general signal input circuit configuration that was assumed in the original telemetry system design is shown in Figure 2.3-2. The EMP filters (see Section 2.4) were designed for low impedance loads to minimize the possibility of ringing and EMP coupling on the gauge cable signal lines. Under these conditions, the nominal 3-dB point of the EMP filter response is 10 kHz (and typically 11 to 12 kHz in actual practice) and rolls off at about 12 dB/octave, so is the limiting factor in system frequency response. An analysis was made by Dr. R. A. Shunk, Appendix B, of the effects of the bandwidths and digitizing rates, used in this system, on typical stress gauge data and both were judged to be satisfactory for the application.

For common mode rejection, the operational amplifier input is nominally balanced and represents a 100 kilohm load from each line to ground for common mode signals. In fact, the degree of unbalance is principally determined by differences in EMP filter components used in both lines. However, it is estimated that common mode rejection will always be greater than 30 dB under the conditions described. The active load (see Section 2.2) the operational amplifier represents to differential signals can be as low as 25 kilohms so the source impedance should be less than 200 ohms to avoid errors in gain, which is nominally unity. The full-scale analog input to the amplifier is ±10 volts peak and digital full scale is 5 volts, due to folding discussed in Section 2.2, so both signal level and dc offsets should be considered when defining the gauge circuit scale factors. Note that the amplifier will withstand input voltages up to ±25 volts; this provides additional protection.

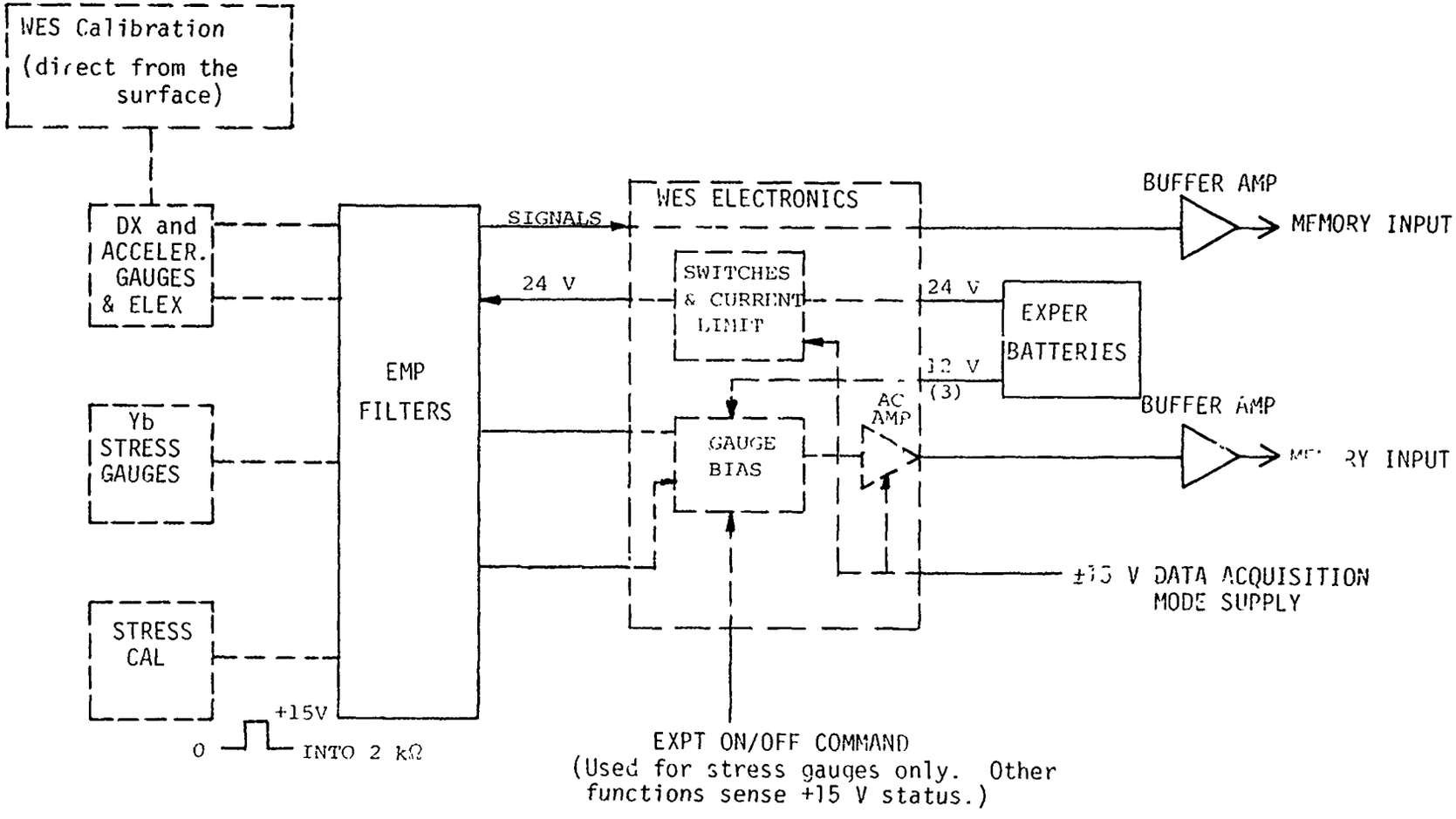


FIGURE 2.3-1
EXPERIMENT INTERFACE BLOCK DIAGRAM

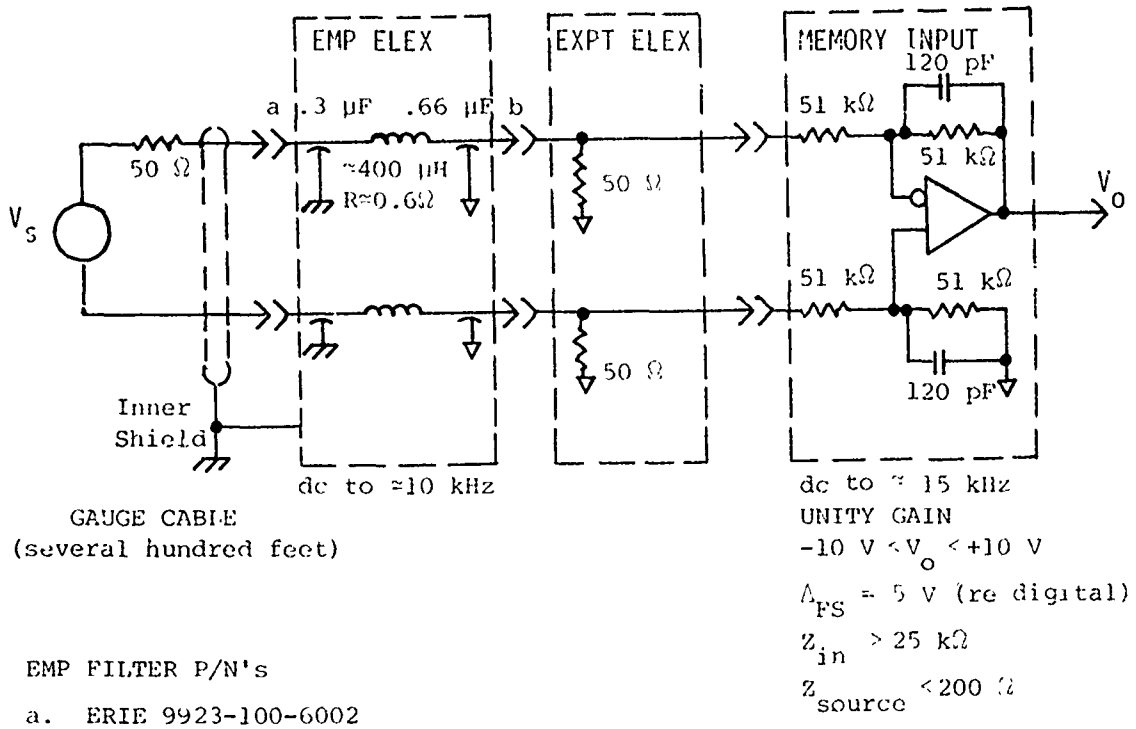


FIGURE 2.3-2

IDEAL SENSOR INPUT CIRCUIT CHARACTERISTICS

The experiment electronics can be located either internally in the telemetry system, as suggested in the ideal circuit, or externally with the gauges - both were done in the Mighty Epic application. However, it is clear from the discussion above that the experiment electronics impedances and signal levels will have a significant effect on system response and must be considered in detail. Because of time limitations in preparing the experiment electronics for Mighty Epic, it was necessary for WES to use a standard velocity gauge design, a standard type of accelerometer design and a modification of existing stress gauge circuits. Although the results were not optimum, it was decided, after a review of EMP, signal amplitude and frequency response, by DNA that they would be acceptable.

The DX velocity gauge electronics, for example, has a 1 to 1.5 kilohm output impedance and is designed to drive 5 volts into 300 ohms full scale.

Tests with the EMP filters and the equivalent source shown in Figure 2.3-3 resulted in a 3-dB bandwidth of 375 Hz, and it is expected the bandwidth would be approximately 250 Hz for a 1.5 kilohm source. (Ringing, particularly for long lines, was not evaluated.) However, the velocity gauge excitation is believed to be 3 kHz and only a 300 to 500-Hz data bandwidth was expected so the results are compatible. An analysis of the effects of this condition on typical data was done by Dr. R. A. Shunk, Appendix C, who concludes reconstruction may be advisable for signals with rise times less than 3 milliseconds.

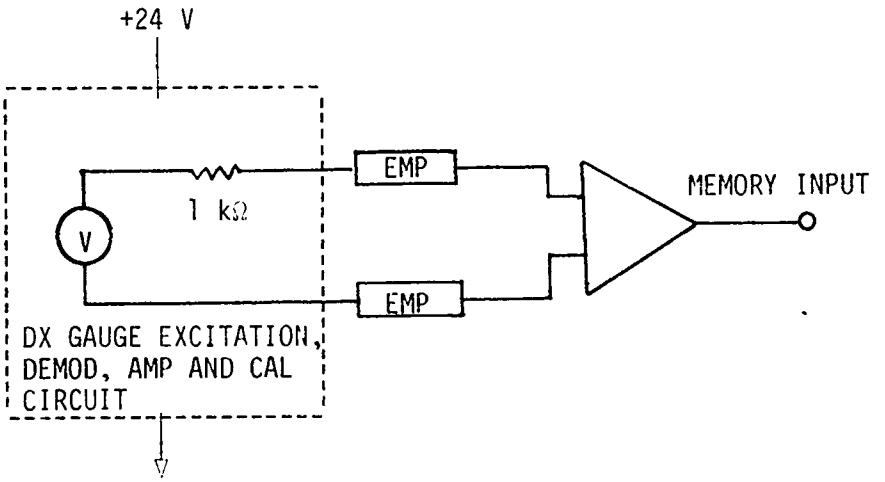


FIGURE 2.3-3
DX VELOCITY GAUGE EQUIVALENT CIRCUIT

The accelerometer circuit, Figure 2.3-4, is a voltage source at low frequencies and has a net output impedance of two hundred ohms (assuming a gain of approximately 100) at 10 kHz. Tests on the EMP filter with a low impedance (50 ohm) source in parallel with one kilohm and an open circuit output show the filter response is still on the order of 10 kHz. Also, the pulse response ringing appeared negligible, but this was not evaluated with long lines. However, since the output impedance of the 5556 amplifier is rising rapidly at the higher frequencies, it is likely the accelerometer input circuit bandwidth was somewhat less than 10 kHz. (This may not have been a factor with the actual data.) Large signal slew rate limiting of the amplifier resulting from having to drive the relatively high EMP filter capacitance of 0.5 μF may be a more significant

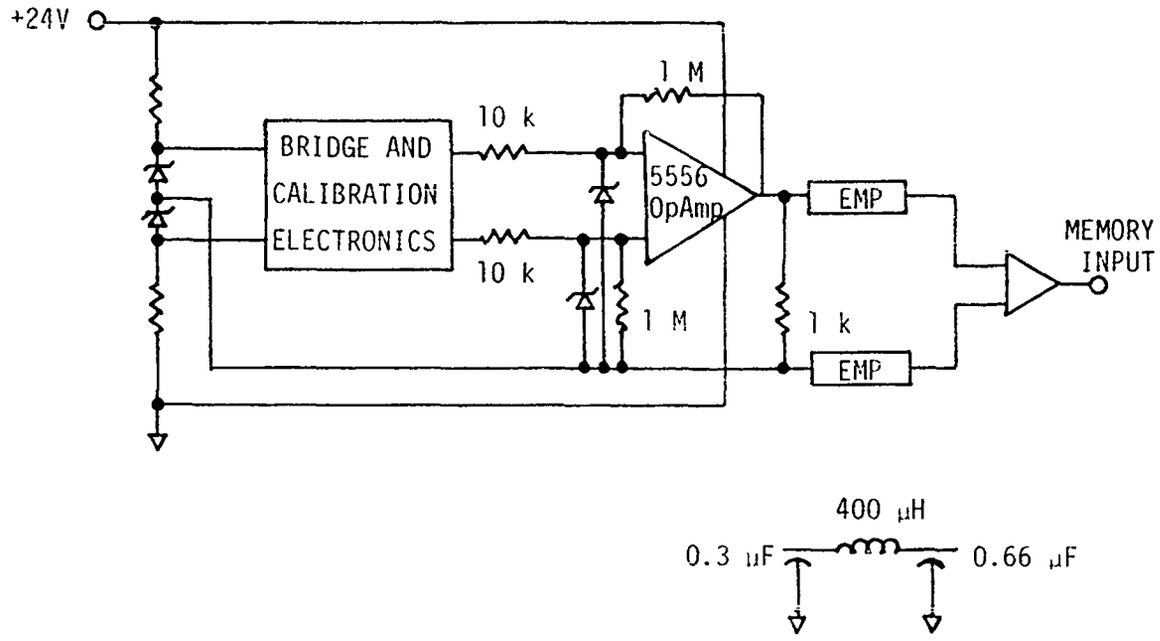


FIGURE 2.3-4
ACCELEROMETER ELECTRONICS SIMPLIFIED CIRCUIT

constraint. Since the amplifier current limit is typically on the order of 20 mA, the maximum slew rate could be as low as 0.05 V/μs or less. Note the presence of the 12-volt common mode signal, due to the reference tap in the supply circuit, is acceptable.

It was not possible to evaluate the DX and accelerometer circuit effects in detail in the system due to severe time limitations. Laboartory tests were limited to the rough equivalent checks described above and a functional check of the memory input. Preshot calibration tests were conducted by WES and it is believed that behavior was normal for their requirements.

The basic Ytterbium stress gauge circuit was a 100 mA constant current type designed for 50-ohm gauges by Stanford Research Institute (SRI). It was necessary for WES to modify this circuit to provide a calibrate function and add an ac-coupled amplifier to remove offset and provide some gain, for the Mighty Epic application, as shown in Figure 2.3-5.

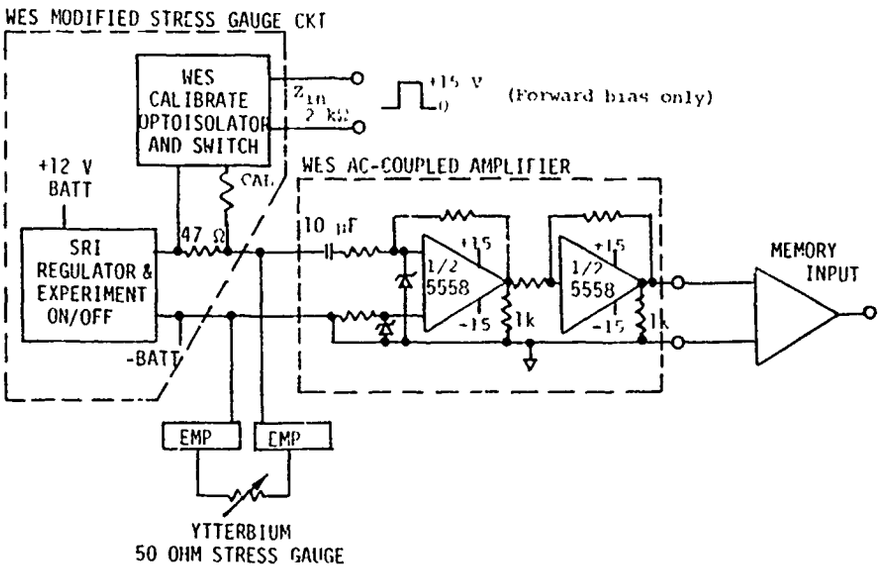


FIGURE 2.3-5

STRESS GAUGE ELECTRONICS SIMPLIFIED CIRCUIT

It is believed the amplifier input time constant was on the order of several seconds. Although no frequency response measurements were made, the 3-dB rolloff of the EMP filters is still on the order of 10 kHz with the 50-ohm stress gauge and high impedance amplifier input as shown by the equivalent measurements described above.

The actual stress gauges were not available for testing, but rough checks were made in the laboratory, with an arbitrary 50-ohm load, to verify circuit operation and the results are given in Table 2.3-2 for reference. The stress gauge channels were found to be sensitive to noise which is probably due to the connection of the amplifier negative output (and experiment battery minus) to telemetry circuit ground. Gain and high level signal response were checked by driving a signal through a 10-dB, 50-ohm precision attenuator, measuring canister input and memory output (except for Canister No. 1 where memory input was measured). The cali-

TABLE 2.3-2

STRESS GAUGE CHANNEL CALIBRATION CHECK

UNIT	GAIN CHECK			CALIBRATE OUTPUT
	INPUT Volts p-p	OUTPUT Volts p-p	APPROXIMATE GAIN V/V	Volts p-p
CANISTER #1 (210') Ch 4A	1	8	8	1.8
Ch 5A	1	4	4	1.2
CH 6A*	-	-	-	-
CANISTER #2 (300') CH 4A	4	22(est)	5.5	1.3
CH 5A	2.5	20	8	1.9
CH 6A	2.5	19	7.6	2.0
CANISTER #4 (400') CH 4A	1.5	24(est)	16(?)	1.8
CH 5A	3	17	5.7	1.6
CH 6A	3	16	5.4	1.2

All dynamic measurements made at 100 to 200 Hz, R_L=54Ω and V_{BATT} ≈13 V.

*Channel 6A ac amplifier DOA.

bration output was similarly measured except the WES calibrate circuit was driven with a 0 to +15 V square wave. The intended gain and calibration step for each channel is not known but the results appear reasonable.

Stress gauge bias (quiescent) was measured for reference as shown in Section 2.3.2. Note that it varies with battery voltage and is no longer a constant current source. Also note that the battery voltage will appear on open circuit gauge connector pins, even when the experiment is off, due to to transistor leakage since the internal terminating resistors were removed to provide the calibrate function, but it will not support current and shorts cannot hurt the batteries. WES made detailed preshot calibration tests, including signal polarity, during and after installation.

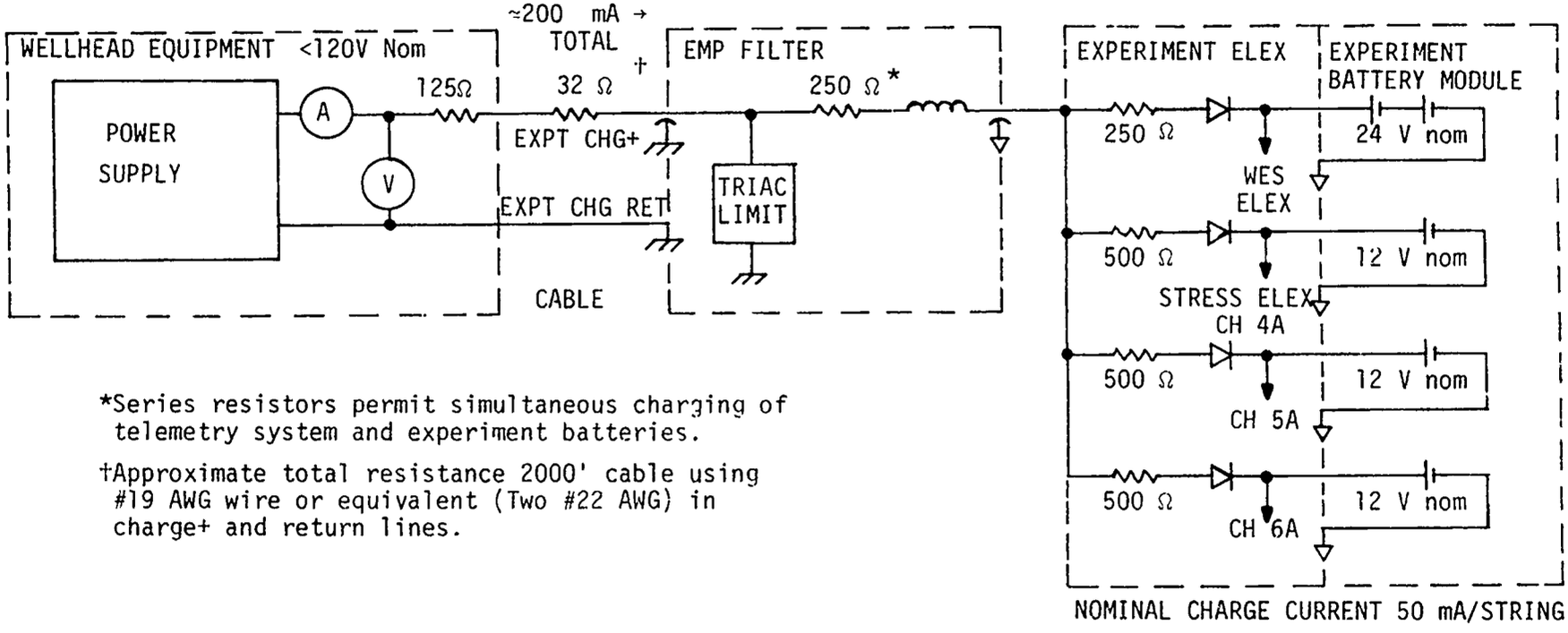
2.3.2 Experiment Power

Experiment power is supplied by a dedicated module of batteries to prevent the loss of telemetry system power in the event of failures in the external gauge cables. Five rechargeable nickel cadmium batteries, nominally rated at 12 volts and 500 mA-hr each, of the same type used for telemetry system power, provide 24 volts for the velocity and accelerometer gauges and individual 12 volt sources for each stress gauge. (Independent stress gauge supplies were originally chosen to insure isolation between channels. Although this feature was not utilized on Mighty Epic, all batteries were retained to insure adequate capacity.) The following is a summary of the final performance and problems in the experiment section; the battery characteristics are discussed more fully in Section 2.5.

2.3.2.1 Charging

The circuit for charging the batteries, Figure 2.3-6, is designed to provide full charge in 14 to 16 hours at the recommended rate of 50 mA. Because of cable and hardware limitations, it was necessary to charge the batteries from a common source that might include simultaneous operation with the much higher voltage telemetry batteries (see Section 2.5 and Section 2.6 for additional charge circuit details). Thus, a series of power resistors were used to provide a distributed drop of the much higher power supply voltage to experiment battery levels and to approximately balance the charge current between the four battery strings. The ac-coupled Triac circuit is designed to provide additional EMP protection for the experiment circuits by shunting spurious signals greater than several volts at frequencies higher than a few kilohertz. The details of the pi EMP filter section are the same as for the signal inputs discussed in Section 2.3.1.

Note that the battery voltage can be checked remotely by reducing the current to a threshold value of approximately 100 microamperes which is just sufficient to cause diode conduction in the lowest string, normally a 12-volt battery, unless the 24-volt string is deep discharged. The input voltage, which includes an insignificant series resistor and diode drop of approximately 0.1 to 0.2 volts, is essentially a measure of battery voltage. The voltage of the other strings could be checked



*Series resistors permit simultaneous charging of telemetry system and experiment batteries.

†Approximate total resistance 2000' cable using #19 AWG wire or equivalent (Two #22 AWG) in charge+ and return lines.

FIGURE 2.3-6

EXPERIMENT BATTERY CHARGING CIRCUIT

by slowly raising current and determining the changes in slope indicating conduction in successive strings and calculating voltage, but this generally was not necessary in practice. The experiment batteries charged uniformly under normal conditions as shown by the typical module test charge data, Table 2.3-3.

TABLE 2.3-3

TYPICAL EXPERIMENT BATTERY MODULE TEST CHARGE DATA

(arbitrary charge status)

PRECHARGE VOLTAGE	CHARGE AT 200 mA TOTAL		POST CHARGE VOLTAGE
	Initial Voltage	Final Voltage After 1½ hrs	After 40 Minutes
11.69	13.37	13.73	13.37
11.74	13.64	13.79	13.46
11.68	13.43	13.76	13.43
23.38	26.99	27.54	26.83

When fully charged and not under load, individual battery voltage will be 14 to 14.5 volts and settle to approximately 13.6 volts one hour after completing charge. Typical manufacturer's discharge data for the experiment batteries is shown in Figure 2.3-7. Voltage will drop from 13.5 volts to 12.5 volts or 12.2 volts only after one hour of operation at the typical experiment loads of 100 mA to 200 mA, respectively. These figures were confirmed by observation.

Under normal conditions, the internal discharge of the batteries is about 1% per day and a data acquisition cycle consumes approximately 1/2%. Assuming a 1 or 2 day delay since the last full charge, and 1 or 2 calibration checks, the most probable operational battery voltages under the nominal loads in this experiment are 13.5 volts if fully charged and 12 to 13 volts even after numerous acquisition cycles and days of unloaded storage in the lab under these conditions. However, there were interface complications which prevented attainment of this

goal on several channels in the final systems as described below.

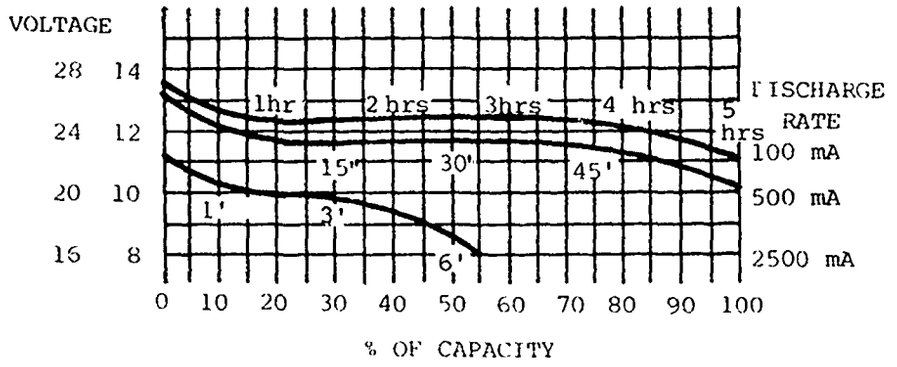


FIGURE 2.3-7

TYPICAL EXPERIMENT DISCHARGE CURVES

2.3.2.2 Loads

24-Volt Gauge Power

The nominal 24-volt supply current requirements for the WES gauges and associated electronics are 12 to 14 milliamperes for accelerometers and 18 to 20 milliamperes for velocity gauges. Since there are a total of nine such gauges per system, a total design load of 180 milliamperes was used to insure some margin. Therefore, about 0.5% of the battery capacity is used per acquisition since the total power-on time is about 60 seconds. It is understood that gauge circuit operating characteristics change and problems start to occur below 19.5 volts, so that 20 volts is a minimum practical operating voltage. Details of the cabling to the WES gauge canisters are not known, but assuming three separate #22 AWG pair circuits up to 300 feet in length, the maximum line drop will be on the order of half a volt. Thus, approximately 21 volts at the canister terminals is a conservative minimum operating voltage.

The methods used to switch and limit the 24-volt buss power are shown in Figures 2.3-8 and 2.3-9. In the original design, which was installed in Canister #4 (400'), WES had used a 24-volt regulator ahead of the switch. Unfortunately, this configuration causes a continuous 6 to 10 milliampere drain on the 24-volt batteries in the standby mode which completely discharges the batteries in a few days. Because of the drain, the operational battery voltage would probably be 24 volts even if peak charge is

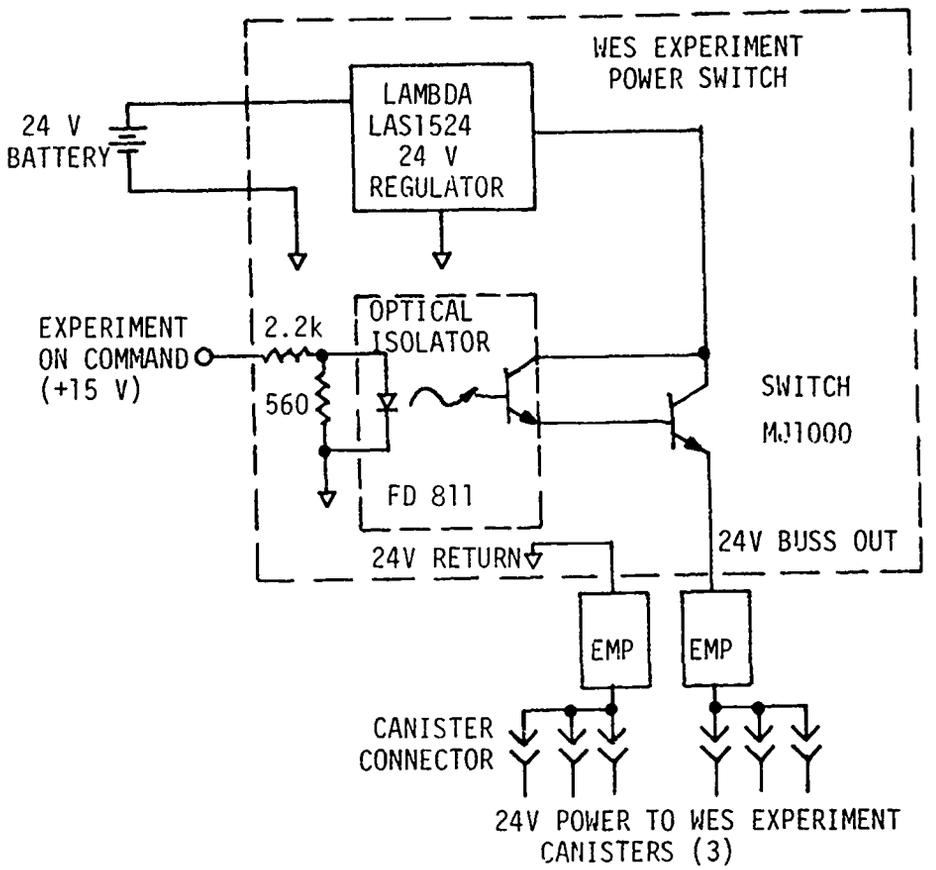


FIGURE 2.3-8

24 V WES EXPERIMENT POWER CONTROL WITH REGULATOR
CANISTER #4 (400')

reached, with a normal preshot standby time. System test data taken with nominal battery voltage on Canister #4, Table 2.3-4, shows the canister output voltage will meet the WES minimum requirements with a nominal battery voltage. Note that the regulator is not in an operating regime and the reduction in output voltage results from the approximately 3-volt drop across the regulator and switch.

Another problem results from the inability to independently charge the stress gauge batteries which means they will be considerably overcharged, with some risk of damage, before the 24-V batteries are fully charged. However, it can be seen from the discussion of battery charging considerations in Section 2.5, that the risk is relatively small if the batteries are allowed to normally remain in the discharged state, test charge time is minimized, and a full charge is only run just prior to lockout. (Charging at shot time was prohibited.) Note that deep discharge at relatively low currents is not likely to damage the batteries. Since this condition was discovered at final system tests (because time did not permit prior experiment integration) and the unit was needed for emplacement, DNA personnel decided to accept these operating constraints for Canister #4.

The circuit was modified to eliminate the regulator and add a current limiting circuit, as shown in Figure 2.3-9, for the remaining two units.

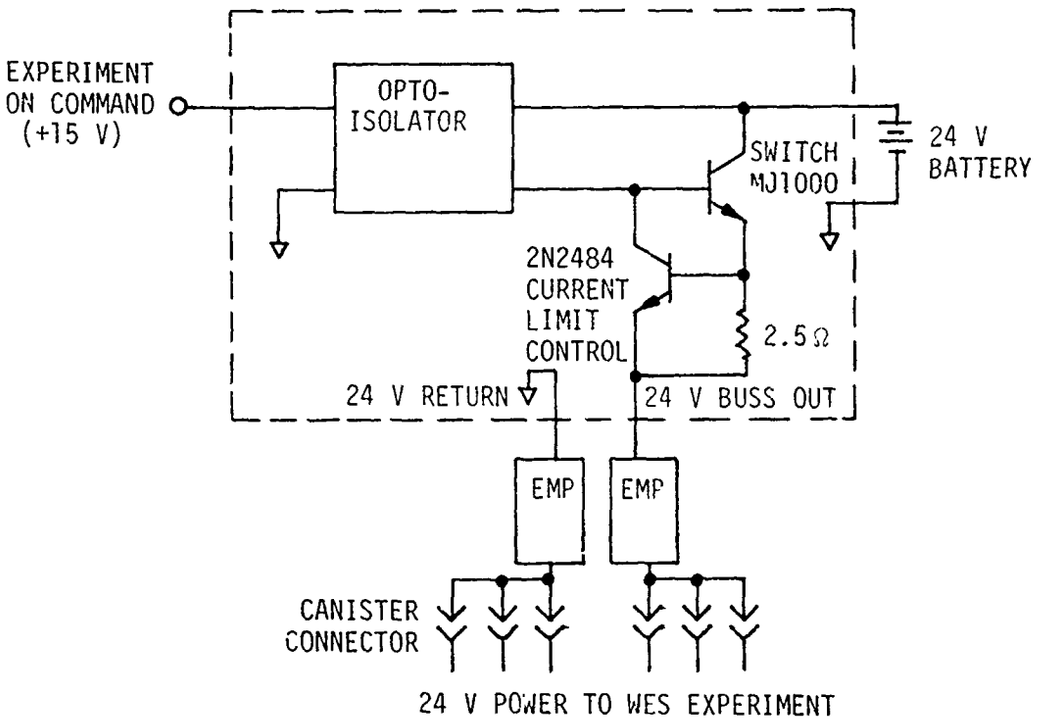


FIGURE 2.3-9

24 V WES EXPERIMENT POWER CONTROL WITH CURRENT LIMIT

CANISTER #1 (210') & #2 (300')

The circuit output was designed to roll off, then limit at about 250 mA, as shown in Figure 2.3-10, for protection in the event one of the gauge power lines failed. (Fuse links were provided for each of the separate 24-volt buss lines, in the WES junction box, to each of the three gauge canisters. In the event one line shorts, power to the other gauges should return to normal after the fuse blows.) Measured system output voltages, Table 2.3-4, show the operating margins are adequate with this configuration.

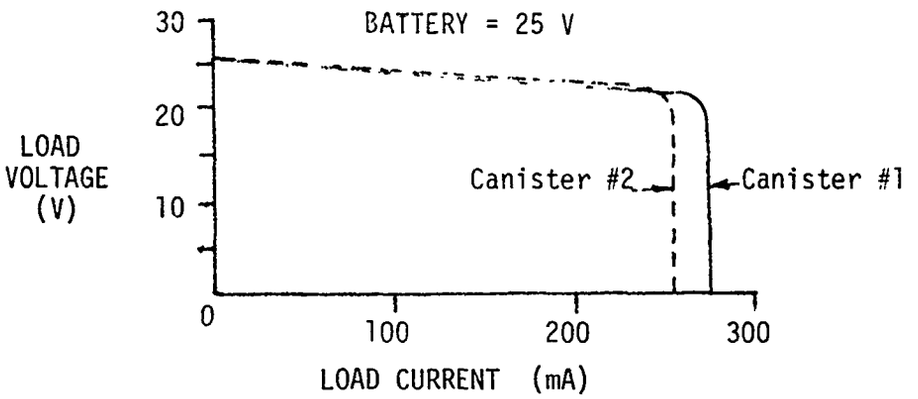


FIGURE 2.3-10

24 V BUSS CURRENT LIMIT CHARACTERISTICS
(Measured at Limiter Output)

TABLE 2.3-4

24 V EXPERIMENT POWER OUTPUT TESTS

(R_L = 130Ω; I_L = 185 mA @24 V)

	210' CANISTER #1	300' CANISTER #2	400' CANISTER #4
BATTERY VOLTAGE (OPEN CIRCUIT)	27 V	26.8 V	24 V*
LOAD VOLTAGE (INITIAL/FINAL)†	24.3/24.2 V	24.0/23.8 V	20.8/20.6 V

*With Regulator Load

†Refers to beginning and end of the Acquisition Cycle.

12 V Gauge Power

The 12 volt batteries were originally intended to supply a constant current of approximately 100 milliamperes into each nominal 50-ohm stress gauge load. Because the bias output of the modified regulator and switch circuitry (Section 2.3.1) was on the order of 6.5 volts, the actual load could be 40% higher, depending on actual gauge resistance, but is still well within the battery capacity limits. System test data taken (see Table 2.3-5) show the batteries provide the proper gauge bias at the canister output in all cases. The open circuit voltage is given for reference - note the drop of approximately one volt that occurs in the circuitry with the experiment on. A charging problem in Canister #1 was caused when the Channel 5A stress gauge (12 V) circuit failed on, during installation, thus constantly draining the battery. As in the case of Canister #4, the only solution was to do a full charge just prior to shot time.

±15 V Power

Because of the late addition of the ac-coupled amplifiers in the stress gauge circuits described above, ±15-volt data acquisition power was supplied by the telemetry system as an expendiency. Normally this would be undesirable due to the goal of achieving complete separation of telemetry system power from the experiment in the event of catastrophic failures on any of the external gauge cables. However, it is permissible if adequate isolation and limiting is provided. A maximum current budget of ±50 mA was available for this purpose and the usage goal was set at ±25 mA to insure reserve. Actual use was not verified, but appears to have been within acceptable limits.

TABLE 2.3-5

12 V EXPERIMENT POWER OUTPUT TESTS

(R_L = 54 Ω; I_L ≃ 120 mA @ 6.5 V)

	APPROXIMATE† BATTERY VOLTAGE	CANISTER OUTPUT VOLTS OPEN CIRCUIT	CANISTER OUTPUT VOLTS WITH LOAD
CANISTER #1 Ch 4A	13.7	12.8	6.5
5A		12.9	6.5
6A		12.9	6.5
CANISTER #2 Ch 4A	13.6	12.5	6.6
5A		12.3	6.5
6A		12.2	6.4
CANISTER #4 Ch 4A	N/A*	11.9	6.0
5A		12.0	6.0
6A		12.0	6.0

All voltages measured with experiment on.

†Minimum string voltage at time of test.

*Battery voltage not measured but probably less than 13 volts.

2.3.3 Experiment Power Up Commands

The telemetry system powers up its data acquisition mode power supplies and provides power up commands to the experiment when the system receives a Ready command. The Ready command was chosen to be T-25 seconds, the maximum allowable in this application, to permit adequate time for stabilization prior to the start of the acquisition process. Data acquisition (i.e., digitizing and storage) starts upon receipt of a FIDL (T=0) command. The experiment is powered down when the telemetry system powers down (to standby) which is normally 30 seconds after FIDU so the total experiment-on time is about 55 to 60 seconds. (If there is no FIDU command, power down occurs at 30 seconds after Ready.) Note the system will not respond to any further commands during the time it is in the acquisition mode until after it has powered down. However, the accidental repetition of both a Ready and a FIDU command after that time will cause the previous data to be written over.

The actual system experiment-on command function is designed to drive several optical isolator switches in series, when separate experiment supplies are used, as shown in Figure 2.3-11. When Ready occurs, the experiment command function transistors sink the +15 V acquisition supply to "ground", through the optical isolators by providing a constant current source of 18 ±2 mA with a voltage compliance of +5 to +15 volts on the Experiment On/Off (-) buss The external optical isolator diodes provide a bypass in the event of isolator failure and are normally shunted by the internal diodes. This command was used on the stress gauge boards which had a separate battery for each channel. The WES functions only required one switch so the +15 volt acquisition supply, which comes on at Ready, was used directly to drive an optical isolator, as shown in Figure 2.3-8.

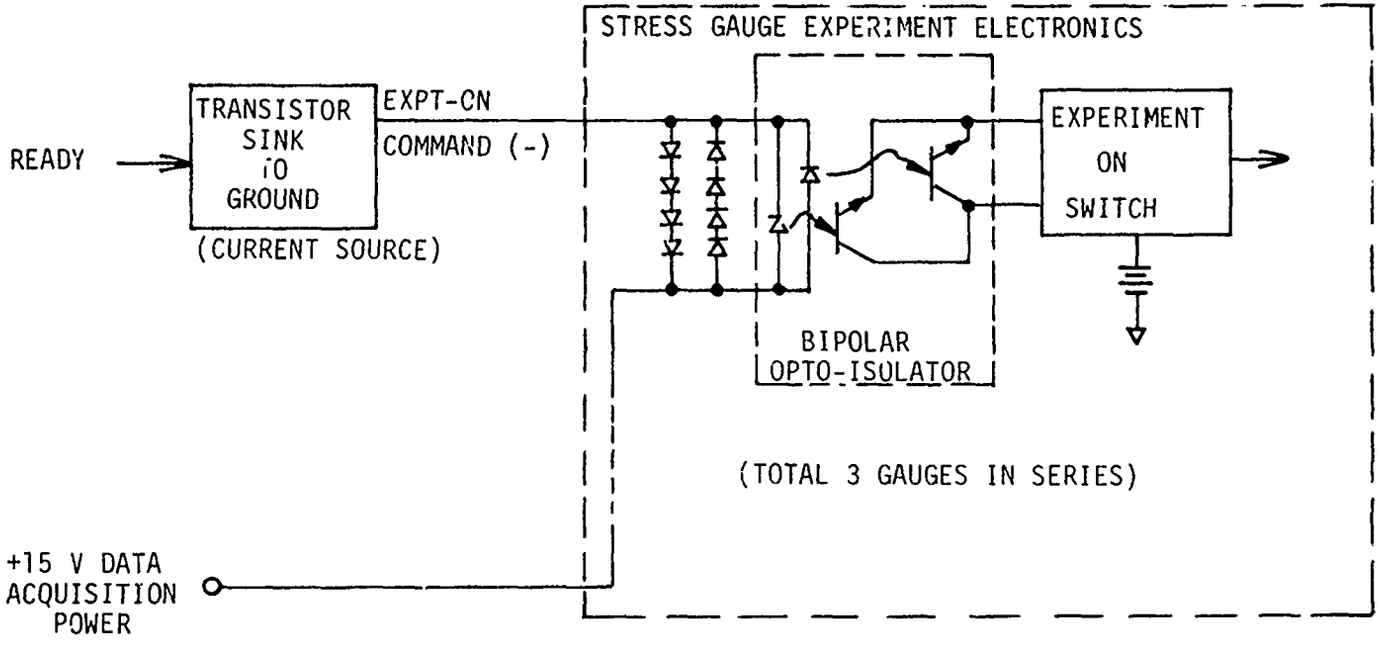


FIGURE 2.3-11

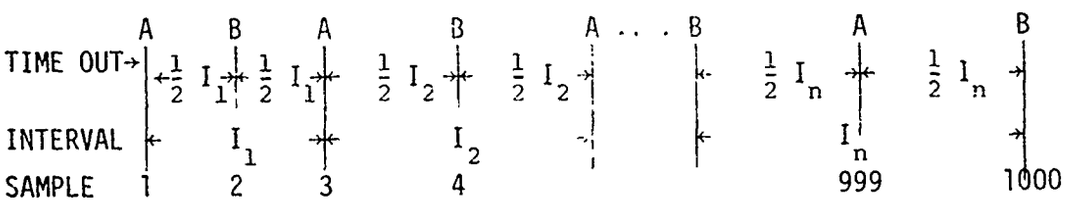
EXPERIMENT-ON COMMAND FUNCTION

2.3.4 Experiment Data Sampling and Storage Format

The data acquisition parameters are preprogrammed in PROM memory and external Ready and FIDU commands are required to start acquisition as discussed in Section 2.2. A time out from FIDU to the start of data sampling can be set from a minimum of 52 microseconds to a maximum of 200 milliseconds. Both channels of each pair must have the same time out and sample interval.

As currently structured, the sampling rate can be programmed in 12 time blocks. The first two blocks can operate at predetermined sample intervals (for each channel of a pair) of 52 and 104 microseconds, respectively, but with numbers of samples separately programmable from 1 (minimum) up to 127 intervals in each block. In the remaining 10 blocks, both the length and number of intervals may be independently programmed. The length (time between samples) may range from 156 to 6708 microseconds in steps of 52 microseconds, and any number of intervals from 0 up to 127 may be specified, in each block. Note, however, that the current memory capacity of 8000 bits per channel pair will be filled after a total of 500 samples per channel.

There is no constraint on the order of sample rates after the first two blocks, but only in these two blocks can the 52 and 104 microsecond intervals be achieved. Also, it is not necessary to use all 12 blocks; the acquisition program may be terminated at the end of any block. Supercommutating a signal, by cross-strapping a pair to a single input, halves the intervals and doubles the number of samples. The samples of each multiplexed channel pair are interlaced. Channel A is sampled first, right at the end of time out and is also the last sample at any given rate except at the end of the program. Channel B is the first sample at each new rate, occurring at one half the new interval (I) after the last A sample, and the last sample at the end of the program; e.g.,



The actual sampling programs selected by WES for the Mighty Epic program are given in Table 2.3-6. In this case, all channels in a given canister have been identically programmed. The programmed acquisition times are plotted in Figure 2.3-12 as functions of stored data location. Note that since all programs are for about one second or greater, all systems were programmed for a maximum of two seconds of digital operation after FIDU (as opposed to 30 seconds of acquisition power supply and analog operation) as discussed previously. (Excess data simply overflows the memory.)

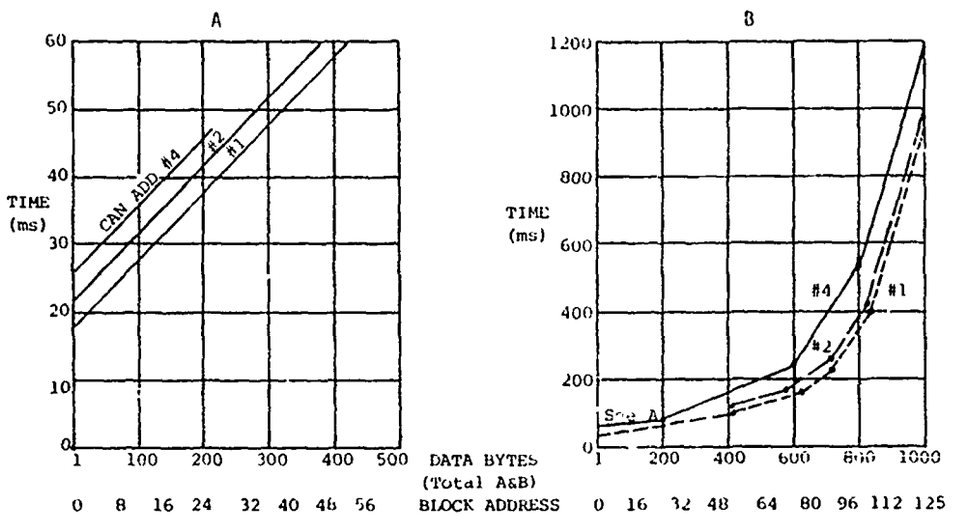


FIGURE 2.3-12
PROGRAMMED ACQUISITION TIME SUMMARY

For transmitting convenience, the data stored in each channel is divided into 125 blocks of 8 data bytes each. Each transmitted byte is an 8-bit data sample word plus parity. The address of the first block is 0 and the address of the last or 125th block is 124. Since there are always an even number of bytes in the transmission of a group of blocks, the first data byte is Channel A and the last data byte is Channel B. The 3 bytes of housekeeping data (a number proportional to the logarithm of current drain with the transmitter on, MPU on and in standby, respectively) that precede each data transmission are not included in data block count. However, they are included in the receiver byte counter display.

TABLE 2.3-6

WES DATA SAMPLING PROGRAM SUMMARY

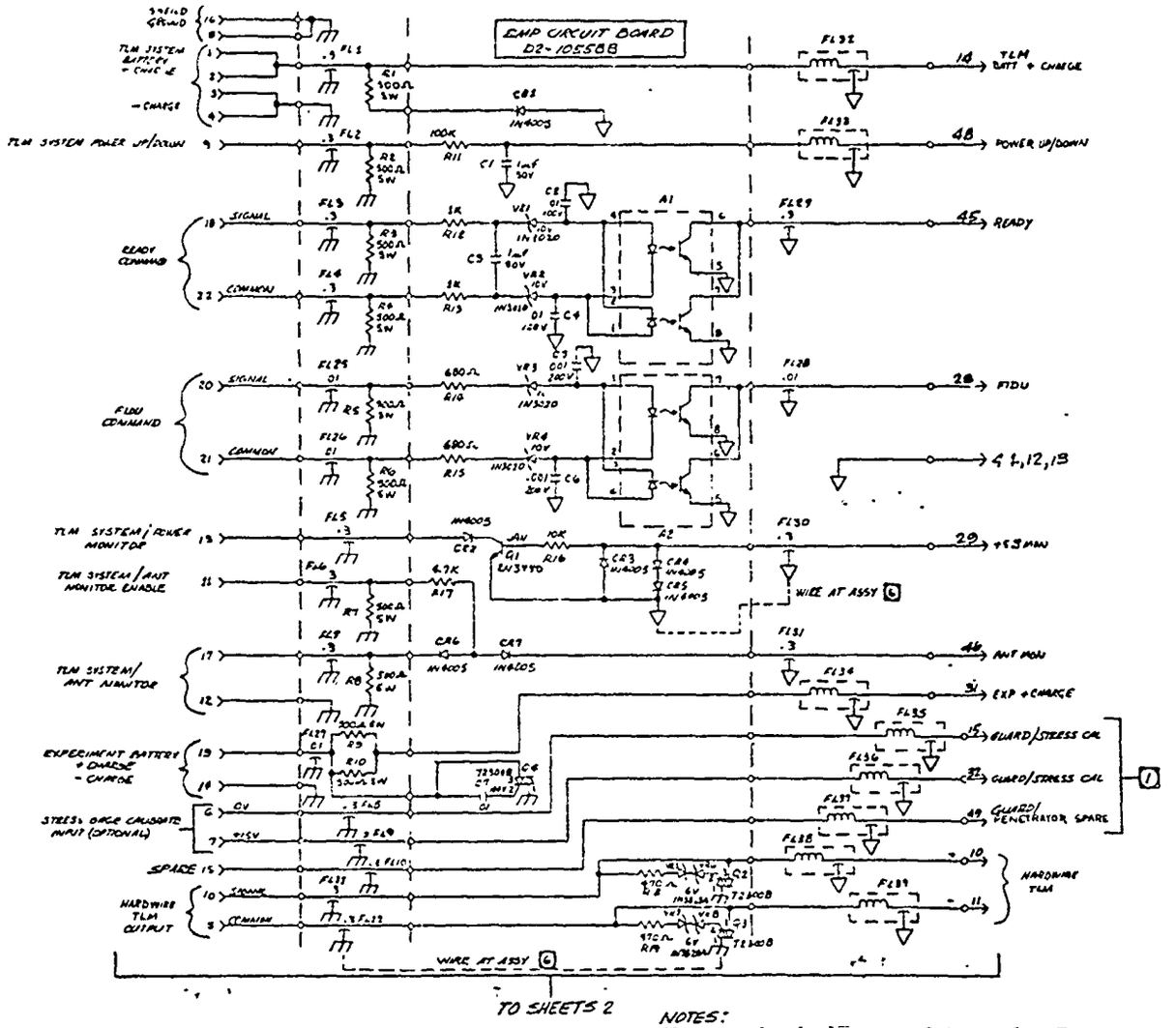
	NOMINAL SAMPLE INTERVAL (each channel-ms)	NUMBER OF SAMPLES (each channel) Ch A	Ch B	CUMULATIVE TOTAL SAMPLES (both channels)	NOMINAL TIME INTERVALS (ms)
HOLE 210', CAN ADD #1	-	-	-	-	Time out 0 to 18.0
	0.052	2	1	3	18.0 to 18.052
	0.104	1	1	5	18.052 to 18.156
	0.028	210	210	425	18.156 to 61.836
	0.832	100	100	625	61.836 to 145.036
	1.664	50	50	725	145.036 to 228.236
	3.328	50	50	825	228.236 to 394.636
	6.656	87	88	1000	3.94.636 to 977.036
		500	500	TOTAL:	0-977.036 ms
HOLE 300', CAN ADD #2	-	-	-	-	Time out 0 to 22.0
	0.052	2	1	3	22.0 to 22.052
	0.104	1	1	5	22.052 to 22.156
	0.208	210	210	425	22.156 to 65.836
	0.832	75	75	575	65.836 to 128.236
	1.664	75	75	725	128.236 to 253.036
	3.328	50	50	825	253.036 to 419.436
	6.656	87	88	1000	419.436 to 1001.836
		500	500	TOTAL:	0-1001.836 ms
HOLE 400', CAN ADD #4	-	-	-	-	Time out 0 to 25
	0.052	2	1	3	25 to 25.052
	0.104	1	1	5	25.052 to 25.156
	0.208	100	100	205	25.156 to 45.956
	0.832	200	200	605	45.956 to 212.356
	3.328	100	100	805	212.356 to 545.156
	6.656	97	98	1000	545.156 to 1194.116
		500	500	TOTAL:	0-1194.116 ms

2.4 EMP PROTECTION

The command and control cable is located very near the working point (and might even pass through it in some applications) so there was considerable concern about protecting the system from the effects of EMP currents that might be induced on the cable shield. Since there is very little published data and great variation in the opinions on the subject, DNA conducted a brief analysis and estimated the worst-case currents to be expected as shown in Appendix D. Originally, the EMP pulse was estimated to be on the order of a kiloampere with a rise time on the order of 100 nanoseconds and a fall time of 100 microseconds, but the rise and fall times were later revised to the order of 0.5 to 1 microsecond and 10 to 50 microseconds, respectively, after further consideration of the actual Mighty Epic configuration.

Because there is some possibility that the EMP currents can couple some energy to the signal lines inside the double shielded cables, the EMP protection and filter circuits shown in Figure 2.4-1 were developed. Actually, the first degree of protection is provided by the system operating philosophy which is to lock out any further commands for 30 seconds once the acquisition process has been started by proper Ready and FIDU commands which would usually precede an EMP pulse. Even if an EMP pulse of sufficient magnitude preceded a tardy FIDU command pulse to the canister on that command line, it would only serve to start the acquisition process regardless of its polarity.

Since system logic operation is relatively immune to EMP-caused disturbances, the main objective in EMP protection became the prevention of high frequency energy spikes from entering the system and causing damage. Thus all lines entering the penetrator section were filtered with shunt capacitance at the first bulkhead. High energy, relatively high voltage is required to operate all monitor, charge and command functions with optical isolators providing additional protection on the critical Ready and FIDU command lines. Further filtering is done at a second bulkhead for all functions including the use of LC filters on the signal lines to provide a low pass frequency response of about 10 kilohertz assuming relatively low impedance terminations. (Additional details on EMP circuit operation are given in other sections of this report.)



NOTES:

1. CAUTION - REFER TO BATTERY CONNECTOR WIRING BEFORE USING (DS-105550)
2. FILTERS 1-12 & 29-31 ARE .8 μF @ 200 WV, 100V, ERIE #2223-100-6002.
3. FILTERS 25-28 ARE .01 μF @ 600V, GUDEMAN 274C103NFT-10
4. FILTERS 32-39 @ 100V, USCC #2121-057
5. PINS 16, 17, 18, 30, 33, 34, 35, 49, 50 & 51 CONNECTOR TO BE USED. SEAL ENDS & SECURE AT COPPER PLATE.
6. REFER TO EMP CIRCUIT BD ASSY D2-105583 AND FILTER CAN ASSY D1-105588 WHEN WIRING MODULE.
7. ALL INTERNAL MODULE INTERCONNECT WIRING IS TO BE #22 AWG TEFLON INSULATION. USE TWISTED PAIRS WHERE INDICATED.

FIGURE 2.4-1A

EMP CIRCUIT SCHEMATIC 6-105588
Sheet 1

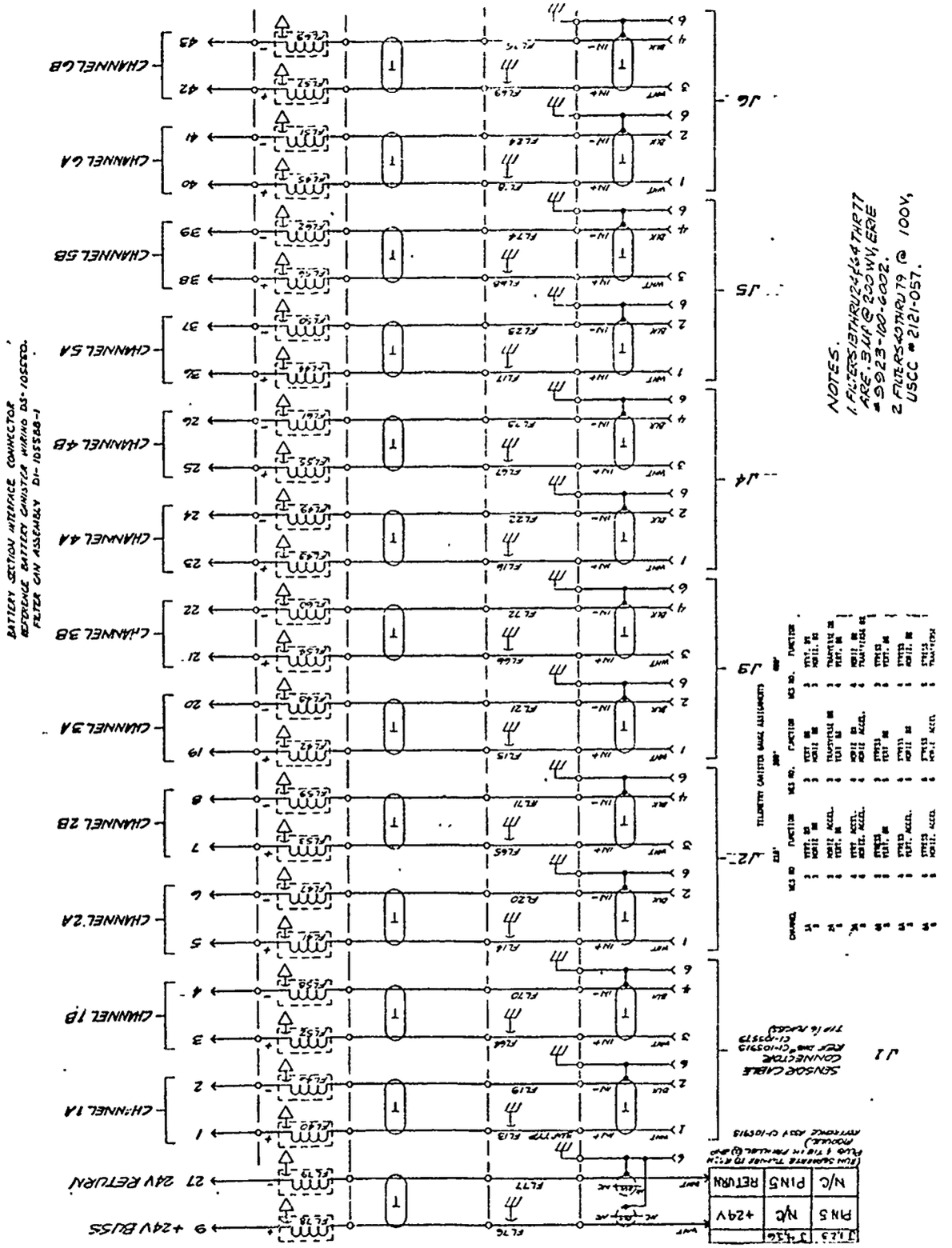


FIGURE 2.4-1B

EMP CIRCUIT SCHEMATIC 6-105588
Sheet 2

In order to determine whether such currents could couple significant levels of interference into the telemetry canister, sample cables and a penetrator section containing EMP filters was tested at Physics International as shown in Figure 2.4-2. Approximately 33 feet of the command and control cable, with separate outer braid shield to simulate the WES conduit, and three signal cables in conjection with the penetrator itself formed the center conductor of the coaxial test configuration. The outer conductor of the coaxial geometry consisted of a cylindrical cage, approximately 12 to 14 inches in diameter, constructed from 1/2-inch diameter conduit. The conduit was connected to the test penetrator mounting flange which in turn was attached to the outer surface of a doubly shielded instrumentation screen room containing recording oscilloscopes. The outer shields of each cable type and one twisted pair line (telemetry plus charge charge function) was driven directly by current pulses up to 1 kiloampere in amplitude and with rise and fall times of about 0.7 microseconds (10-90%) and 43 microseconds (e-fold), respectively.

In brief, the results were as follows:

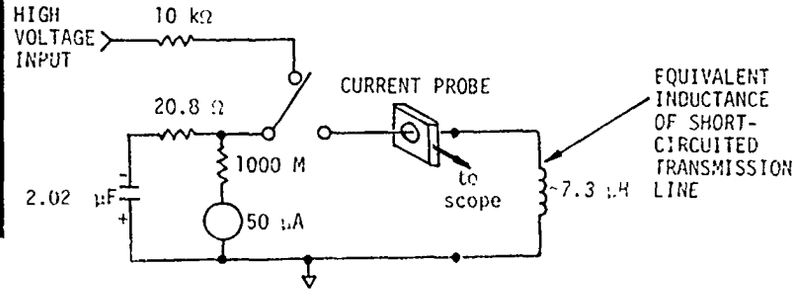
A. There were no signals at any of the EMP filter outputs that were in excess of a 100 mV or so when the cable outer shields were driven with currents up to 1 kiloampere.

B. The signals that were observed may in fact have been due in whole or in part to coupling through the screen room as determined first by shorting the transmission line with the cables disconnected and then disconnecting the transmission return conductors from the penetrator.

C. The ringing characteristic of the signals observed seems to be due to excitation of the 33-foot transmission line.

D. When the telemetry battery charge line was driven directly, coupling to other functions was insignificant at lower levels and never greater than several hundred millivolts even after the capacitor in the driven circuit apparently failed at around 1 kilovolt.

In conclusion, it appears the penetrator design, the connectors and the method of terminating the shields on the cables used in the test do in fact provide adequate EMP protection.



CURRENT INJECTOR EQUIVALENT CIRCUIT

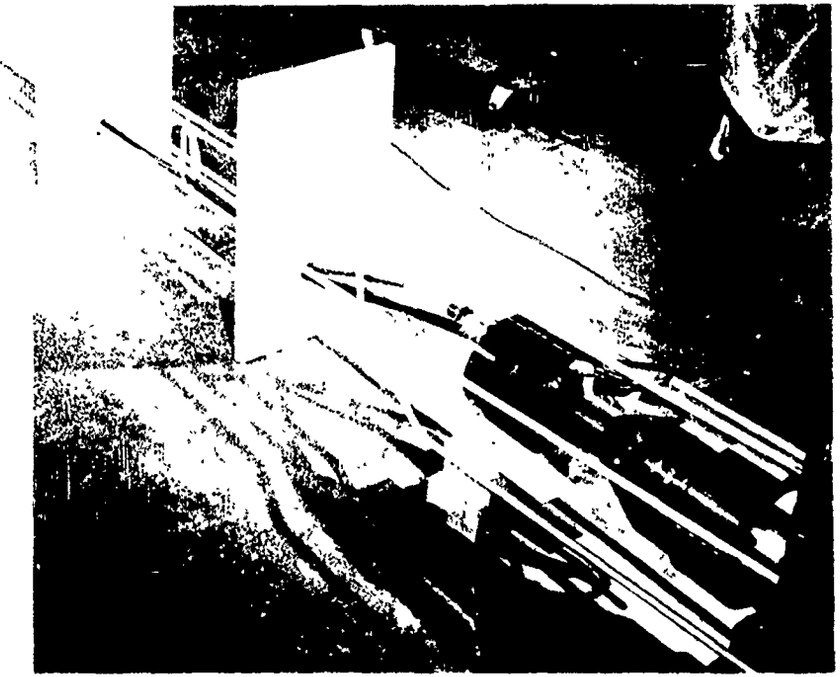


FIGURE 2.4-2
PENETRATOR EMP TEST SETUP

2.5 DOWNHOLE SYSTEM POWER

2.5.1 Batteries

The energy storage in the downhole system must be sufficient to allow several weeks of storage before and after the shot in the event of delays, and more than one complete data dump to permit reverification of data that may have suffered from transmission errors. To achieve these goals, a nominal total capacity of 288 watt-hours or 1.036 MJ was provided by eight independent strings of batteries which allows for some redundancy. A total operating voltage of 72 to 75 volts (nominal) per string was used in order to realize high transmitter efficiency and antenna energy storage requirements. Under the conditions of worst-case theoretical system loads, Table 2.5-1, a minimum of one complete dump of the stored data and 32 days of storage can be achieved at the maximum transmission rate of 4 bits per second. Note that completely redundant data dumps or exclusive operation at lower data rates (e.g., 2, 1, and 0.5 bit/second) are not practical since this reserve capability was intended for limited use during times of maximum atmospheric noise, recording problems, etc.

Actual energy use was significantly lower than the worst case, as shown by the estimates, for Canisters 1 and 4, extrapolated from system current measurements in Table 2.5-2. Also, Figure 2.5-1 clearly illustrates the tradeoff of standby for additional transmission time. These values are approximate at best because of the possible variables, but they are consistent with actual operations where all canisters were found to perform properly after more than one dump and 30 days of storage. Canister 2 was, in fact, operated for 1.5 dumps after 31 days of total standby before failing, which is in direct agreement although no actual system power consumption data is available for further comparison. Note that normal operation ceases when the batteries drop to about 65 V and the regulator voltages drop out of tolerance. However, there is still some energy left since the digital circuitry goes into a hang-up mode and cannot shut the system down (it must be manually powered down if it occurs in test), so transmissions continue for another hour or so until the batteries are totally depleted.

TABLE 2.5-1

SUMMARY OF WORST CASE ENERGY REQUIREMENTS

		V_{BATT} NOMINAL VOLTAGE	I_{BATT} MAX CURRENT	WATTS	ENERGY USE
DATA ACQUISITION (60 s total on time)		81 V*	<650 mA	52.65	3160 J/cycle
STANDBY	ELECTRONICS	75 V	<1 mA	0.075	6480 J/day
	BATTERIES (Internal dissipation at ≈1% per day)				10368 J/day
	TOTAL				16848 J/day
TRANSMIT	MEMORY ELECTRONICS, ETC.	75 V	<90 mA	6.75	6.75 J/s
	TRANSMITTER	75 V	<380 mA	28.5	28.5 J/s
	TOTAL	75 V	<470 mA	35.25	35.25 J/s

*Initial Voltage assuming recent full charge

ENERGY USE EXAMPLES
(in joules)

	ACQUISITION	TRANSMISSION	STANDBY	TOTAL
One transmission @4 bps 32 days total standby	3160	499,669	533,971	1,036,800
1.5 transmissions @4 bps 16 days total standby	3160	749,503	284,137	1,036,800
One transmission @2 bps 2 days total standby	3160	999,337	34,303	1,036,800

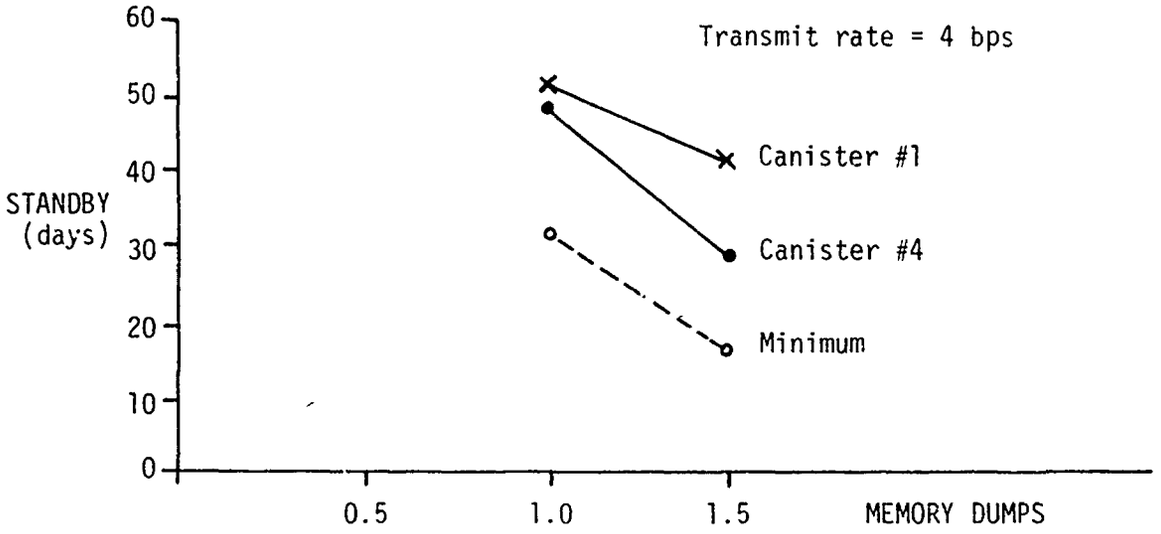
One dump of 6 memories with 8 k bits of stored data each requires transmission of approximately 56,700 bits including parity bits and about 5% overhead (preamble and housekeeping) for multiple (not redundant) interrogations.

TABLE 2.5-2

ACTUAL ENERGY REQUIREMENTS

		CANISTER #1				CANISTER #4			
		V_{BATT} [1] volts	I_{BATT} amps	P_{BATT} watts	ENERGY USE [3]	V_{BATT} [1] volts	I_{BATT} amps	P_{BATT} watts	ENERGY USE [3]
DATA ACQUISITION (60s)		81	0.455	36.86	2211 J	81	0.396 [2]	32.08	1925 J
STANDBY	ELECTRONICS	75	0.96 mA	0.072	6221 J/day	75	0.65 mA	0.049	4212 J/day
	BATTERY @.75%/day[4]				7776 J/day				7776 J/day
	TOTAL				13997 J/day				11988 J/day
TRANSMIT [4] @4 bps	MEMORY CKTS,etc.	75	0.07	5.25		75	0.065	4.87	
	TRANSMITTER	75	0.21	15.75		75	0.365	27.38	
	TOTAL	75	0.28	21	297,675 J/Dump	75	0.43	32.25	457,143 J/Dump

NOTES:
1. Assume recent full charge
2. Extrapolated to 6-channel case
3. Assume total capacity of batteries is 1,036,800 J
4. Estimate for system ambient ≈60°F
5. Assume 56,700 bits transmitted for dump including parity and overhead functions



ASSUMPTIONS: a. One Data Acquisition Cycle

b. Fully charged batteries to nominal capacity of 1.0368 MJ

c. 56,700 bits transmitted per dump including parity and overhead functions

FIGURE 2.5-1

STANDBY TIME vs DATA DUMPS

The batteries used in the telemetry system are sealed sintered-plate nickel cadmium button cell types, with a 12-V, 500 mA-hr nominal rating manufactured by SAFT America (formerly Gulton) under catalog number 10VO-.500SSCP. Ten internally welded cells are molded in epoxy to form a battery approximately 1.5 inches in diameter by 4.34 inches long (3.81 cm dia x 11.02 cm), weighing about one pound (0.435 kg), that will withstand the severe shock levels required in this application. They are rated for use at temperatures between -28°C to +50°C although typical operating temperatures were 15°C to 24°C (60°F to 75°F) in this application. Note exposure to temperatures greater than 50°C should be avoided since the cells may fail - usually short. Eight strings consisting of six batteries each (see Figure 2.5-2) were used to supply the telemetry system power. Diodes were used to isolate the strings from each other and to keep battery voltage off the downhole cable charging circuits.

2.5.1.1 Normal Charging

A battery of this type must receive a minimum recharge of 50% more than the amount discharged. Thus, a fully discharged unit must receive a minimum recharge of about 750 mA-hour. The recommended charge rate is about 10% of the nominal discharge rate so normal charging for a discharged battery would be 50 mA (except under low temperature conditions) for 14 hours - which should give full charge and 1.4 to 1.45 V per cell - to 16 hours - where the battery starts to warm up and there may be a slight lowering of cell voltage. If the cell voltage started out very low, it should come up to 1.4 V per cell after 1 hour or less under charge. If there is a load on the batteries while charging, the cell voltage should still be about 1.4 V, but charge time will be proportionately longer, of course, if the total input current from the charger is 50 mA. After terminating a complete charge, the battery voltage will drop to and stabilize at 1.36 V per cell, open circuit, in about one hour.

2.5.1.2 Continuous Charging

The batteries will take a trickle charge of 12 mA continuously without harm. Continuous charging at 50 mA on a fully charged battery is considered risky, but there are no statistics. It can probably be done for extended periods of time although it is unlikely the batteries will take 50 mA indefinitely. One effect is that carbonate impurities occur in the cell which reduces capacity by approximately 25%; not a major problem in this system.

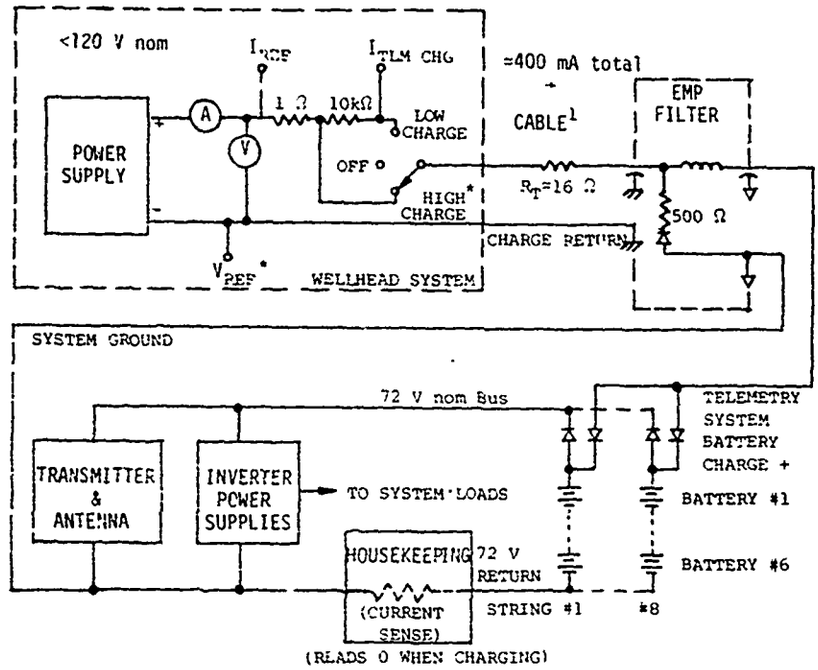
There is also the possibility of creating shorted cells due to the overpressure created because they are not vented. It takes about 2 to 3 atmospheres of gas (200-300 kPa) before heat starts to be generated (about 2 to 3 hours at 50 mA for the 500 mA-hr cell). Due to the thermal mass of the batteries it takes another couple of hours before the battery warms up. The risk of extreme overpressure starts when it is possible to feel the batteries get warm. The fact that the batteries are potted in metal retaining structures which have

good contact with adjacent canister structures adds to the thermal mass and probably extends the process by several times. Gassing is reduced at higher temperatures because cell voltage goes down which reduces the oxygen given off by the plate, thus slowing down the process somewhat. (The converse is also true and it is for this reason the cells should never be charged at 50 mA under low temperature conditions.) Reducing the charge current and increasing the charge time will lower the risk. Thus, it appears probable that the batteries, as used in this system, can survive a 14-16 hour overcharge, as was necessary in two cases for the experiment batteries, particularly if they are allowed to partially discharge (by self or by operation) before the necessity arises.

2.5.1.3 Charging Circuit

The telemetry system battery charging circuit, Figure 2.5-2, was designed to charge all batteries simultaneously; thus simplifying the hardware and minimizing the cable requirements. Diode isolation is used to insure battery voltages do not appear on the downhole cable and to insure some separation of the parallel battery strings. Although parallel charging has some potential problems, there were no practical effects in this application. Note that system operations might entail simultaneous charging of the experiment batteries. Thus, it is necessary to consider the condition of the lowest battery set and possibly do a brief low current precharge to equalize voltages before commencing a full current system charge. See Sections 2.3.2 and 2.6 for additional charge circuit details.

To start a charging operation the battery voltage is checked by increasing the power supply voltage until a threshold current of about 0.1 mA is reached. This is sufficient to cause diode conduction in the lowest voltage battery string. The cable input voltage, which includes an insignificant series resistor and diode drop of approximately 0.1 to 0.2 volt, is therefore approximately equal to the battery voltage. The charge current can then be increased as slowly as required to allow the battery string voltages to equalize. A constant current charge of 50 mA per battery string, i.e., 400 mA for telemetry and 200 mA for experiment batteries, fully charges a completely depleted battery set in about 15



NOTE: 1. Approximate total resistance 2000' (600 m) cable using #16 AWG wire or equivalent (4 #22 AWG) in charge+ and return lines.

FIGURE 2.5-2

TELEMETRY SYSTEM BATTERIES AND CHARGING CIRCUIT

hours. The power supply voltage will be about 10 to 30 volts higher than the battery voltage during charge depending on the exact contact and line losses in the system.

Note that the resistive load in the EMP filter does not affect normal charging since the back biased diode has a 600 V breakdown rating. (This provides additional protection against the possibility of sharp high level EMP interference by loading negative spikes and clamping positive spikes at around 600 V.) The details of the pi EMP filter section are the same as for the signal inputs discussed in Section 2.3.

2.5.1.4 Discharge

Typical manufacturer's discharge data (see Figure 2.5-3) shows that individual battery voltage will drop from 13.5 V, after one hour of operation, to 12.5 V for 100 mA load and 12.2 V for 200 mA load. Voltage then stays at about 12 V to 12.5 V until about 80% of the battery capacity is used, after which it starts to drop. Since the telemetry system drain is less than 100 mA per battery, the most probable system operating levels are 81 V during acquisition (assuming a recent full charge) and 75 V during standby and transmission. A minimum of 65 V is required for proper system operation and is considered the end of nominal battery capacity. It is also important to note that the batteries have a self-discharge, resulting from internal leakage, ranging from typical values of 3/4% at 15°C (60°F) to 1.8% at 27°C (80°F) of total capacity per day which is a significant factor in system standby time.

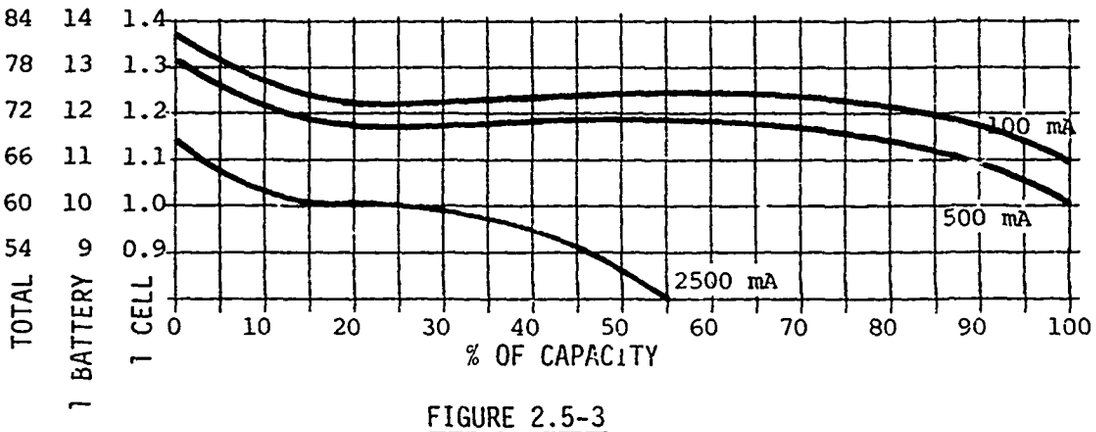


FIGURE 2.5-3

TYPICAL BATTERY DISCHARGE CURVES

Cell reversals, resulting from the fact that cells have different capacities (or they would not occur), are possible after the batteries are discharged below 0.9 V per cell (approximately 9 V at the terminals). However, reversed cells are not necessarily catastrophic and will return to normal after charging under most circumstances. Note that momentary shorts on the batteries may cause cell reversals but should not result in a permanently damaged shorted cell, i.e., it will recover after charging. A dead short would probably have to last as long as three or four minutes to permanently short the cell. Also, the risk of shorting a reversed cell with a continuous load of less than 6 mA is very small, but the risk would become significant with continuous loads up around 50 mA.

2.5.1.5 Battery Tests

Since voltage and capacity are fairly critical in this application, all batteries were tested prior to use (see Figure 2.5-4). Since the batteries were shipped in a discharged condition, they were all charged at 50 mA for 15 to 16 hours. Initial and final voltages were checked before and after the start and completion of charge to verify the conditions described above were met and there were no shorted cells. The batteries were then discharged at a rate of about 120 mA for about 4 hours (values depend upon test condition parameters) until the equivalent of 500 mA-hr had been reached. Initial discharge voltage and currents had to be normal and the final battery voltage greater than 10 volts for acceptance.

There were over 200 batteries tested and 88% met the voltage and capacity requirements. Approximately 6% did not quite meet the discharge test but did not have a shorted cell (i.e., voltages were correct) so were not used. Another 4% had shorted cells caused by incorrect handling and use. Only 2% had inadequate capacity and low battery voltage due to manufacturing defects and were replaced.

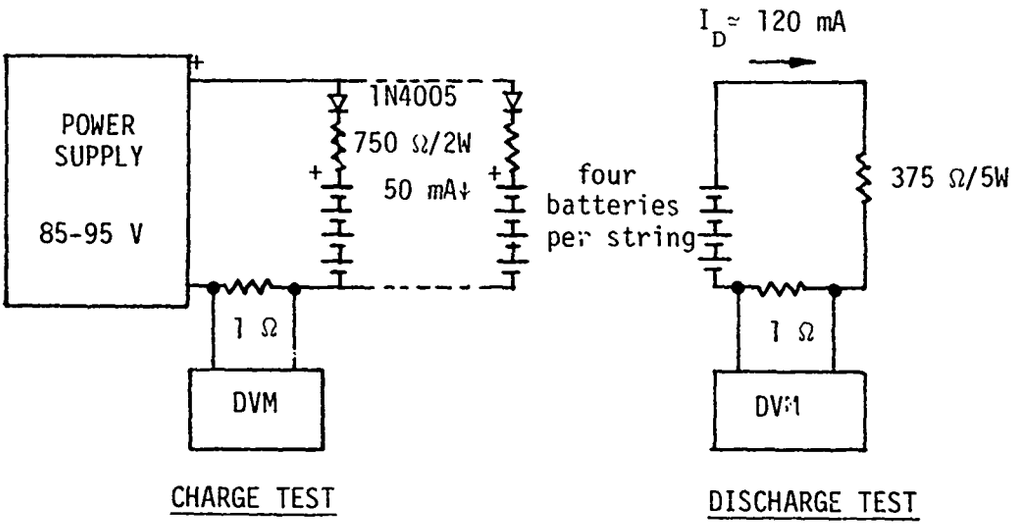


FIGURE 2.5-4
BATTERY TEST CIRCUITS

2.5.2 Downhole Power Supplies

High efficiency dc-to-dc power supplies are used to convert the battery voltage (72 V nominal) to the +5, ±15, and -9 V levels required for electronic circuit operation. Because of the discrepancy in the power requirements of each operating mode (standby, acquisition and transmit), separate supply circuits were used to achieve maximum efficiency. However, the supplies are functionally interrelated and, in some cases, supply common loads through diode coupling and switching networks as shown in Figure 2.5-5. Refer to Table 2.5-3 for requirements.

The standby supply contains circuitry for turning system power on or off by external command. When the system is powered up, the standby supply is always on to provide power to the command logic in the other supplies as well as the RAM memories and acquisition/dump command decoders, etc. The other two supplies are turned on and off by internal system commands generated in response to receipt of valid external acquisition or dump commands.

2.5.2.1 Standby Supply

This supply provides approximately 30 milliwatts of 5-volt power to the canister during all modes of operation. The regulator also provides a 3.6-volt reference voltage for the data acquisition and transmit power supplies.

A schematic of the regulator circuit is shown in Figure 2.5-6. The circuit is a switching type regulator comprised of Q1, Q2, T1, C5 and CR1. Current feedback for regulation is provided by the differential pair Q3, Q4, and the voltage reference diode ZR1. ZR1 is a specially characterized low current zener diode and exhibits a well defined "break point" at only 50 microamperes of zener current. "ON-OFF" control of the regulator is accomplished by the control circuitry Q5, CR2, R10 through R13, C2 and C4.

Regenerative switching action necessary to sustain oscillation of the circuit occurs in the loop containing Q1, T1, C1, R4 and Q2. An increase in current in the base of Q2 will tend to increase the collector

TABLE 2.5-3

DOWNHOLE SYSTEM REGULATED SUPPLY REQUIREMENTS

MODE	BUSS	V_{BATT}	I_{BATT}	V_{OUT}	I_{OUT}(max)
STANDBY	+5 S	65 V min 85 V max 75 V nom	<1 mA	+5 ±0.1 V	<10 mA
TRANSMIT		Same as above	<90 mA		
	+5 AT & 5 T			$+5.2^{+0.2}_{-0.0}$ V	<475 mA
	-9 AT			-9^{+0}_{-1} V	100 mA
DATA ACQUISITION		Same as above	<650 mA		
	+5 AT & 5 A			$+5.2^{+0.2}_{-0.0}$ V	<3.5 A
	-9 AT			-9^{+0}_{-1} V	<600 mA
	+15 A			+15 ±0.5 V	<270 mA
	-15 A			-15 ±0.5 V	<210 mA

NOTES: 1. Temperature: -10 to +50°C, operating; -10 to +85°C, storage. (power supplies only. System operating temperature was limited to +20 to +40°C to optimize energy storage and prevent any possible battery damage in this application)

2. Power supply ripple was limited to ≈50 mV p-p all busses.

3. Design goal for maximum voltage change during shock: +10%, -5%. (no effects were observed during shock tests)

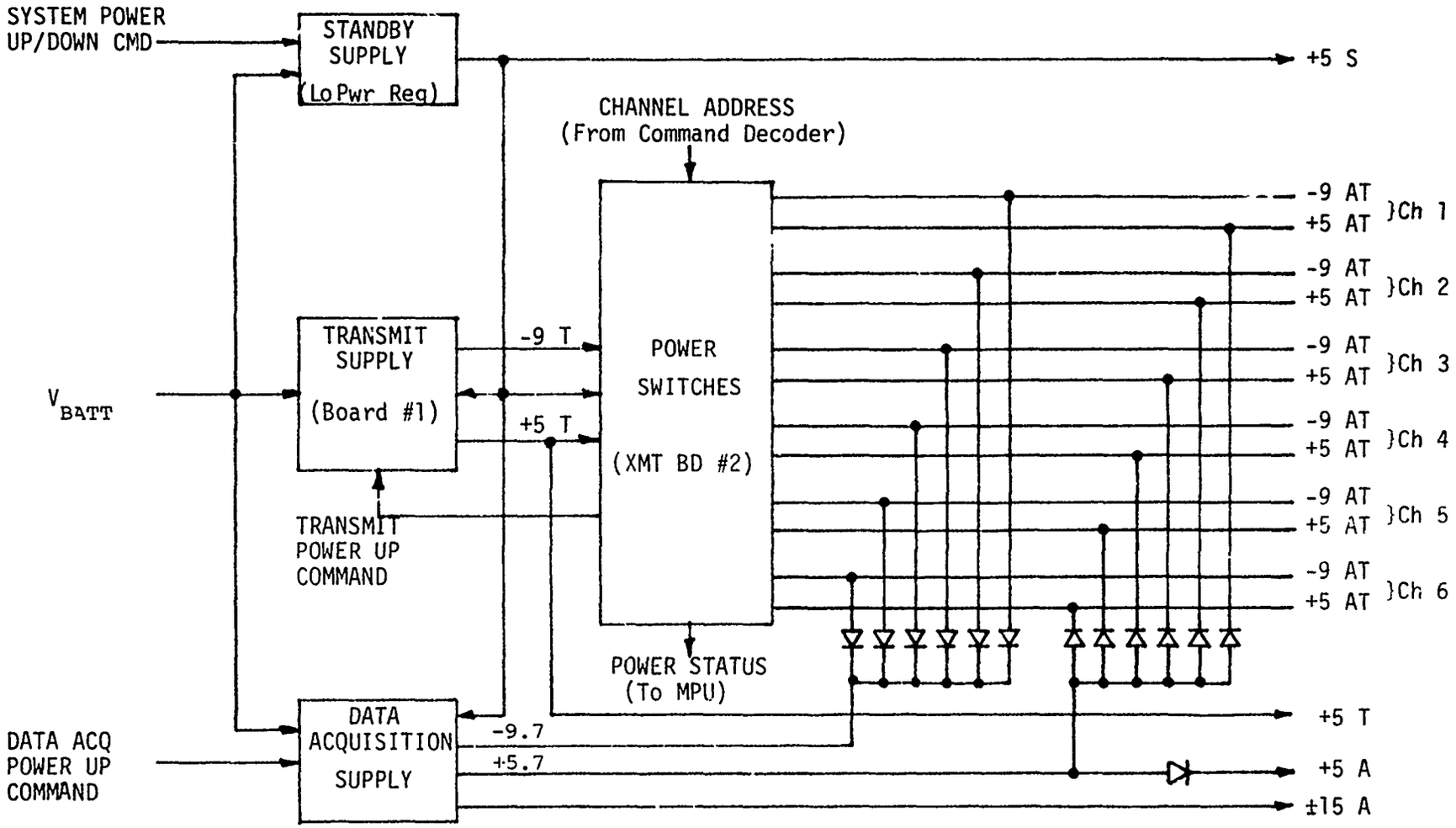


FIGURE 2.5-5

DOWNHOLE SYSTEM POWER SUPPLY BLOCK DIAGRAM

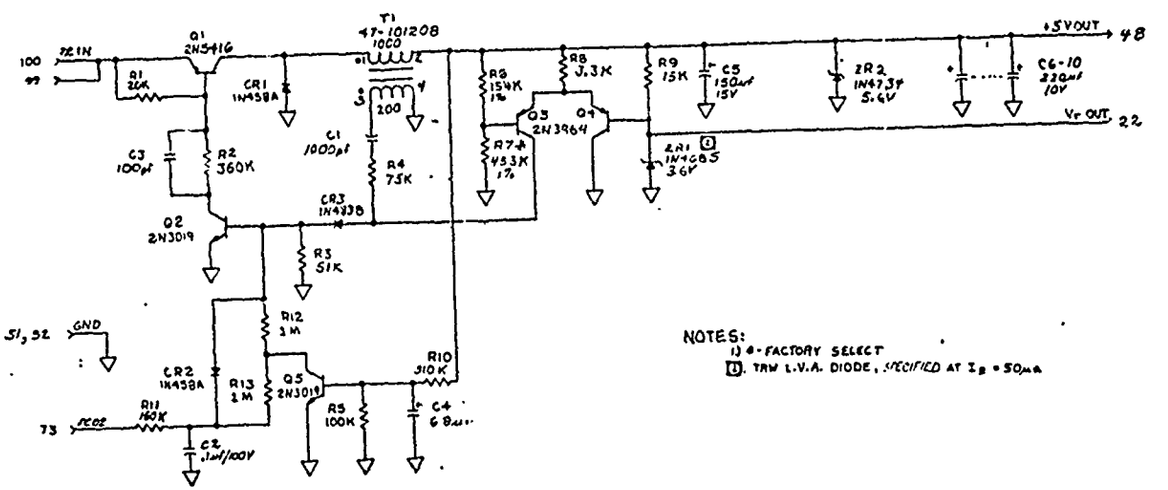


FIGURE 2.5-6

SCHEMATIC, STANDBY SUPPLY BOARD, 105435

current of Q1, thereby increasing the voltage across the primary of T1. This voltage drop is reflected at the secondary of T2, and is of such a polarity as to increase further the base current of Q2 through the feedback network C1, R4. The regenerative cycle continues until Q1 and Q2 are in saturation. At this time a constant voltage appears across the secondary of T1, and the base current of Q2 starts to decrease exponentially at a rate established by the time constant C1 R4. When the base current decays to a value insufficient to maintain saturation of Q1, the switching cycle reverses. The voltage at terminal 1 of T1 then decreases rapidly due to stored current in the transformer primary inductance until it is clamped at approximately zero volts by the commutating diode CR1. Both Q1 and Q2 are now in a nonconducting state and C1 begins to charge in the opposite polarity due to the collector current in Q3. When the voltage at the junction of R4 and CR3 is sufficiently positive to overcome the forward drops of CR3 and the base-emitter junction of Q2, Q2 will again start to conduct and the switching sequence repeats.

The regulator output voltage is determined by the duty cycle of the switching waveform which is established by the magnitude of the collector current of Q3. This current is derived by comparing the reference voltage of ZR1 with a sample of the regulator output voltage from the voltage divider network R6 and R7.

Regulator start up and shutdown is accomplished by applying a bipolar power command to Pin 73 of the module. A positive voltage of about 50 volts on Pin 73 supplies sufficient base current to Q2 through R11, R12, and R13 to insure starting of the regulator. After the regulator has started, Q5 clamps the junction of R12 and R13 to zero volts to prevent a positive voltage on the power command input from interfering with the regulation process. The regulator may be shut down by applying a negative voltage on the same pin whose magnitude is in excess of 40 volts. For shutdown, the clamp Q5 is bypassed by CR2, and sufficient current is stolen from the base of Q2 to cause the regulator circuit to cease self-oscillation. Overvoltage protection due to startup transients is provided by ZR2, which insures that the regulator output never exceeds 5.6 volts.

2.5.2.2 Data Acquisition Supply

The Data Acquisition Supply provides power to all +5 AT and -9 AT lines and the +5 A line during data acquisition modes. In addition, the supply provides positive and negative 15 volts required for analog data acquisition circuitry and some experiment electronics. The supply is designed to provide power as shown in Table 2.5-3.

Power distribution to the +5 AT and -9 AT power busses is made through isolating diodes on the power switching board (Transmit Supply #2). Therefore, the +5 volt and -9 volt outputs to this board are somewhat higher (+5.7 V and -9.7 V) in magnitude to allow for this diode drop.

The circuit (see Figure 2.5-7) is a conventional dc-to-dc converter with voltage regulation applied to the transformer primary. Transistors Q5 and Q6 with transformer T1 form the converter oscillator, which has an operating frequency of approximately 3 kilohertz. Series regulation is achieved in the primary circuit series pass transistors Q1 and Q2, and a feedback error amplifier (Q3 and Q4), which compares the rectified 5.7-volt output with a 3.6-volt reference supplied from the standby supply (low power regulator). The series regulator supplies a constant 65 volts to the dc-to-dc converter.

Power on/off control is provided by a power command (PC-01) from the Control and Timing circuit upon the receipt of valid acquisition commands. The power command controls the state of a SPDT analog switch, a CD4007. When power command PC-01 is low (zero volts), the base of Q3 is clamped to ground, holding the power supply off. A high (+5 V) power command at Pin 64 switches the base of Q3 to the 3.6-volt reference voltage, turning on the supply and providing voltage regulation. The acquisition supply is powered down 30 seconds after Ready or FIDU whichever is later.

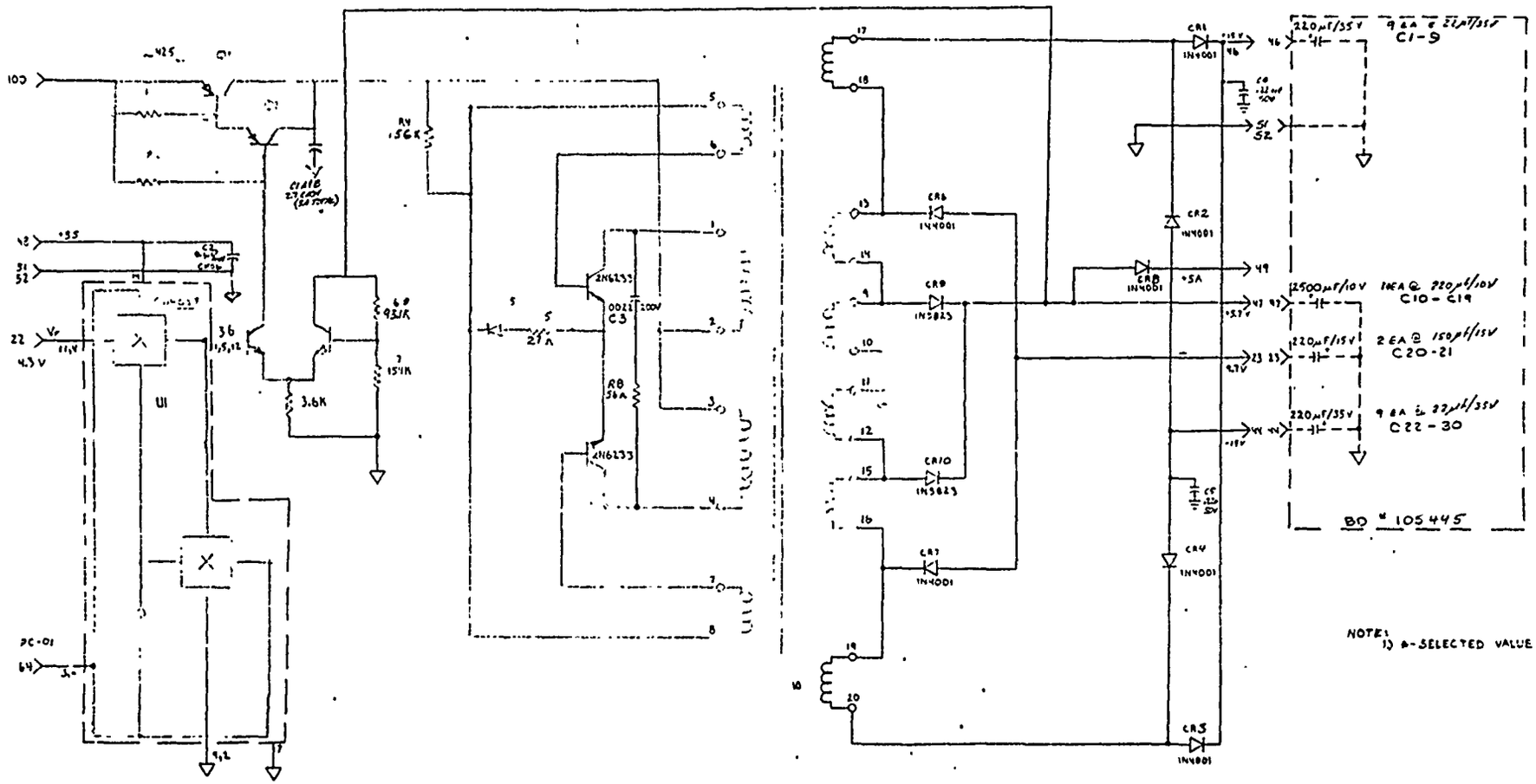


FIGURE 2.5-7

SCHEMATIC, DATA ACQUISITION SUPPLY BOARD, 105443

2.5.2.3 Transmit Supply #1

The Transmit Supply #1 board provides +5 volts and -9 volts to any one of six channels during the data transmit mode. The supply is designed to provide power as shown in Table 2.5-3. Power distribution to individual power busses is accomplished on the power switching board (Transmit Supply #2).

The circuit (see Figure 2.5-8) is a conventional dc-to-dc converter with primary voltage regulation similar to that used in the Data Acquisition Supply (see Section 2.5.2.2). Transistors Q5 and Q6 with transformer T1 form the converter oscillator which has an operating frequency of approximately 3 kilohertz. Series regulation is achieved in the primary by Darlington-connected pass transistors Q1 and Q2, and a feedback error amplifier, Q3 and Q4, which compares the rectified 5-volt output (+5 T) with a 3.6-volt reference supplied from the standby supply (low power regulator).

Power on/off control is supplied by a power command from the channel address decoder on the power switching board. The power command controls the state of a SPDT analog switch (a CD4007). When the power command is high (+5 volts), the base of Q3 is clamped to ground, holding the power supply off. A low (zero volts) power command switches the base of Q3 to the 3.6-volt reference voltage, turning the power supply on and providing voltage regulation.

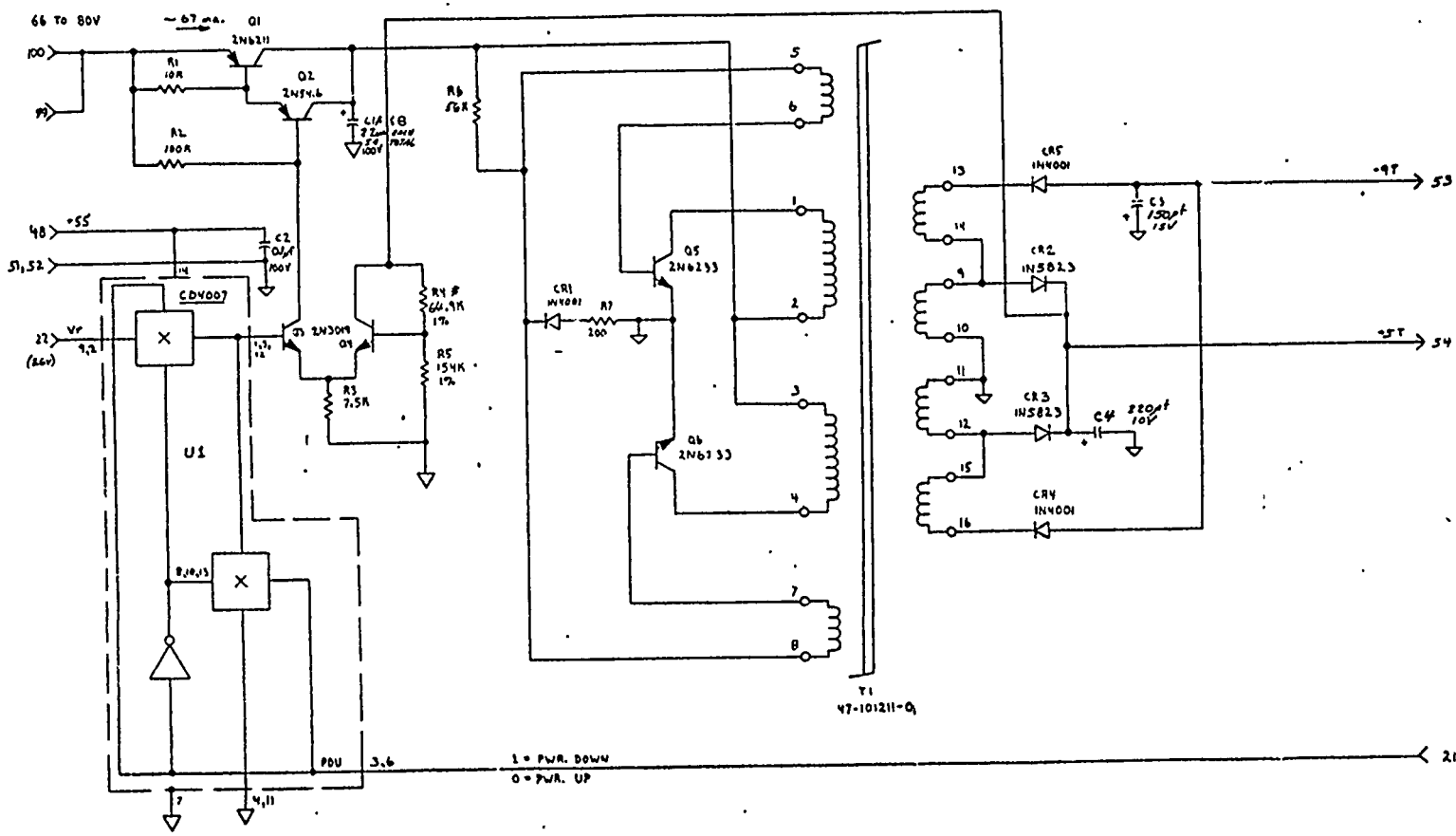


FIGURE 2.5-8

SCHEMATIC, TRANSMIT SUPPLY BOARD #1, 105439

2.5.2.4 Power Switching

This function (Transmit Supply #2 board) controls distribution of +5 volt and -9 volt power to the canister memory channels. The board also generates a "power status" signal to the MPU section which indicates that power to any channel is within tolerance and ready for use. Six +5 volt and six -9 volt outputs are provided. Inputs are +5 V and -9 V power from the Transmit Supply #1 board, +5.7 V and -9.7 V power from the Data Acquisition Supply, and the 3-bit channel address from the receiver decoder.

During data acquisition, +5.7 volts from the Data Acquisition Supply is applied to diodes CR1 through CR6. The -9.7 voltage is applied to CR7 through CR12. Thus, all channels are supplied +5 V and -9 V power simultaneously. In acquisition mode the channel address is <000>. This address causes the power command at Pin 21 to be high, keeping the power converter on Transmit Supply #1 in a power-down state.

The channel address is decoded by U1, a CD4028 BCD-to-decimal decoder. An address other than <000> will cause Pin 21 to go low (zero volts) and bring one of the lines to U2, a CD4050, high to +5 volts. This will turn on one of the transistors in U8, a CA3081 transistor array, and one of the 5V pass transistor switches (Q1 through Q6).

The presence of 5 volts on one of the output lines, Pins 88 through 93, causes one of the level shift transistors (Q7 through Q12) to conduct, thereby turning on the corresponding -9 V pass transistor (Q13 through Q18). The -9 V outputs appear on Pins 24 through 29.

The power status signal (Pin 45) is generated by a zener diode bridge comparator (VR1, VR2, and Q19. Q20 is a level shifter and output logic buffer. C2 provides some time delay to ensure that switching transients on the +5 V and -9 V output lines have settled before a "Power Ready" status signal is applied to the logic output line.

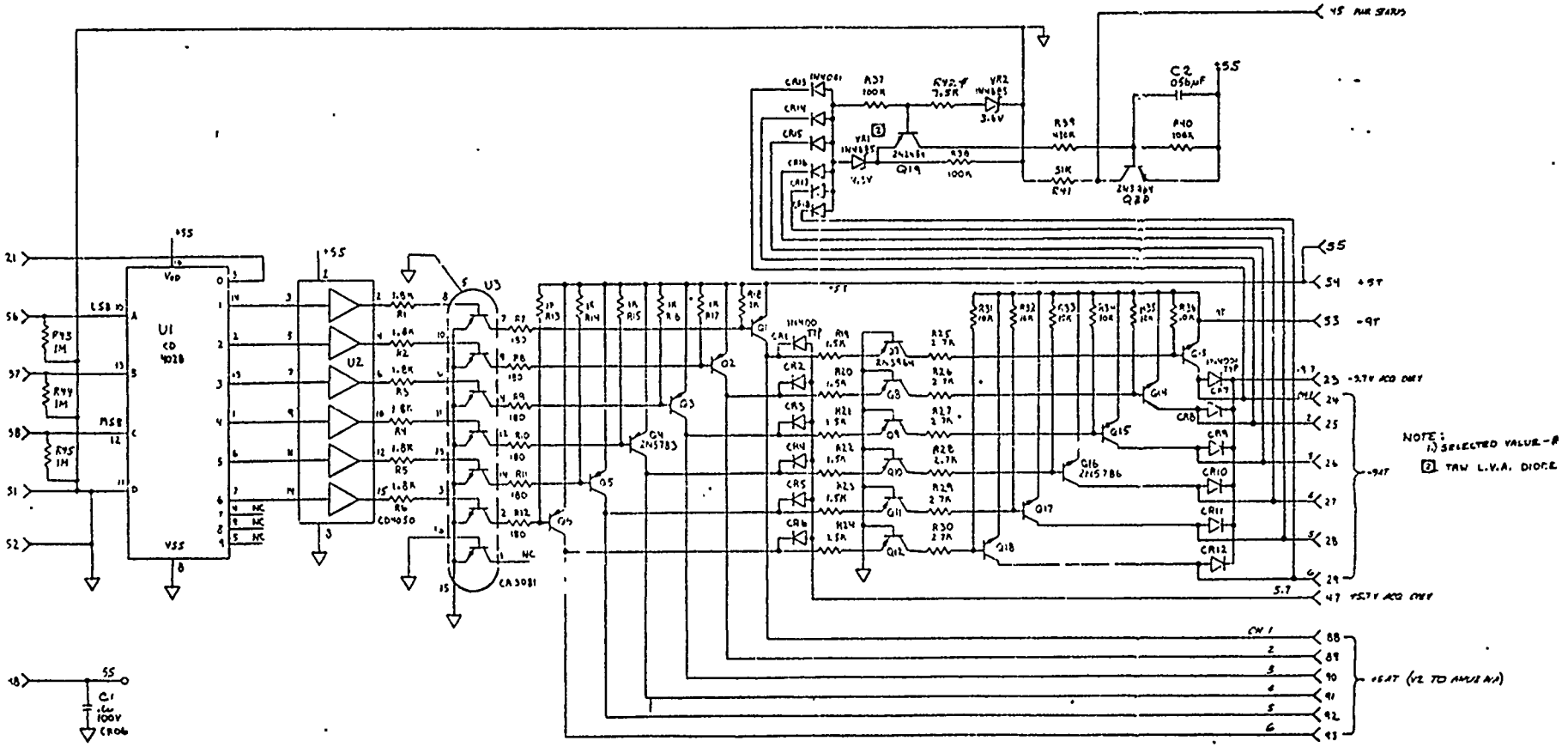


FIGURE 2.5-9

SCHEMATIC, TRANSMIT SUPPLY BOARD #2, 105442

2.5.2.5 Current Sense and Housekeeping

This function monitors the current in the battery return line from the power supplies and transmitter and provides three bytes of data, proportional the the logarithm of the current with transmitter on, MPU on, and standby, at the beginning of each data transmission. Time did not permit refining this circuit to achieve good temperature stability and accurate calibration. but it was useful to provide a qualitative indication of whether system operation was normal. It is recommended that a circuit that provides a cumulative record of charge and discharge energy would be more useful in future systems.

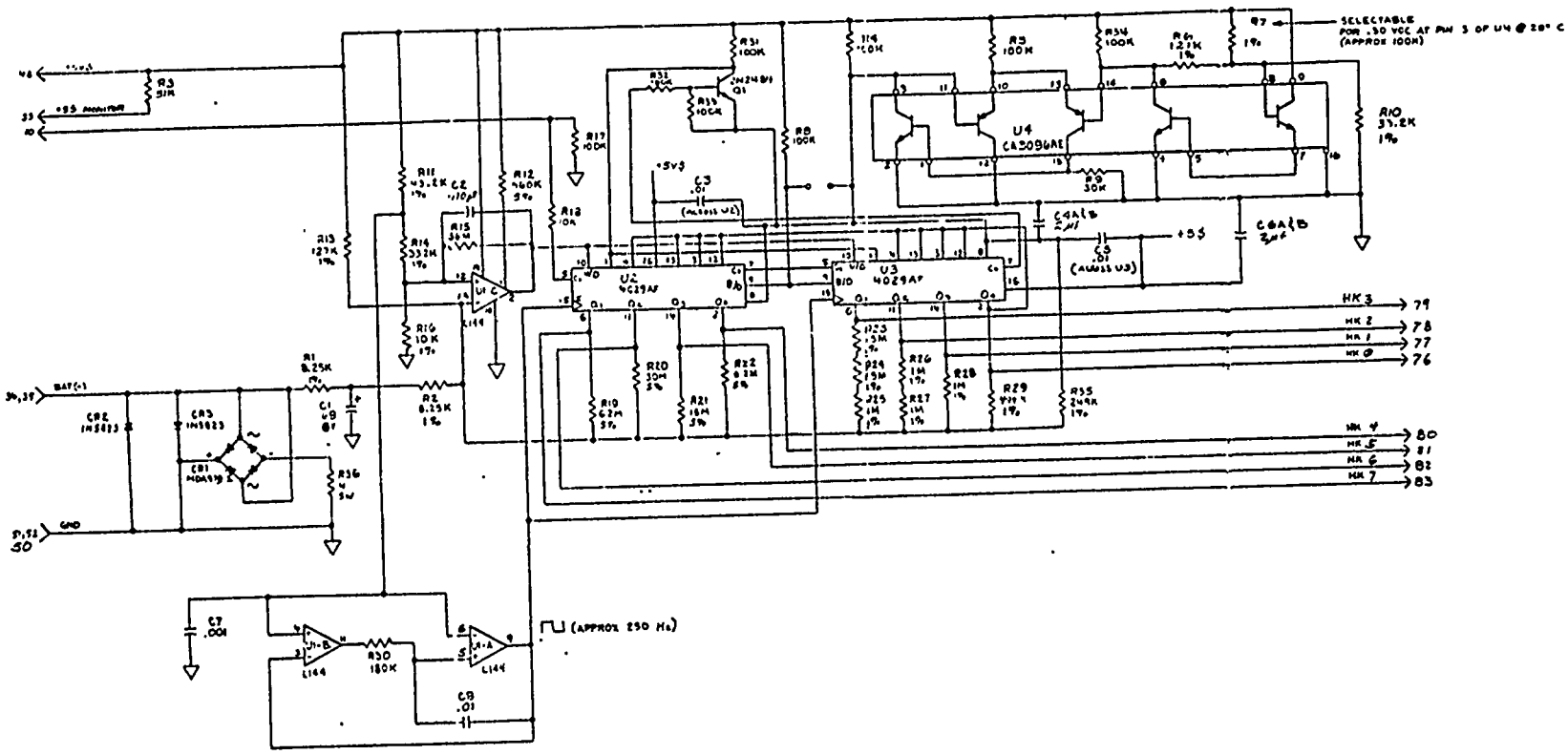


FIGURE 2.5-10

SCHEMATIC, CURRENT SENSE AND HOUSEKEEPING, 105498

2.6 CHARGING, MONITORING, COMMAND AND TELEMETRY ELECTRONICS

These functions include the transmitter and receiver boards in the downhole system and the entire collection of surface equipment, called the Wellhead System. (Strictly speaking, other portions of the downhole system are involved, but they are adequately covered elsewhere.) The Wellhead System provides the electronics for the following functions: (a) to initially charge the downhole canister batteries and monitor various functions, (b) to receive and retransmit the conditioned Ready and FIDU signals (both from the experimenter's electronics or from front panel pushbutton switches for test) that initiate the data acquisition process, (c) RF transmission of an interrogate command word to the downhole canisters, and (d) RF reception of downhole canister data and decoding of this data. Refer to Figure 2.6-1. The Wellhead System is designed to interface directly with up to four downhole canisters (or more on a time-shared basis).

2.6.1 Wellhead Power Supplies

Two power supplies, an HP6443B and an Underground Telemetry Rack Power Unit (Model 105841), are used to power the Wellhead System.

The Model 6443B Dc Power Supply is rated for 0 to 120 Vdc at 0 to 2.5 A. The power supply may be remotely programmed for constant voltage with 300 Ω/V resistance. The input power requirements are 105 to 125 Vac, 57-63 Hz single phase, 6.5 A. The supply is used by the Underground Telemetry Command Transmitter for charging canister batteries, for Power Up/Down control and antenna monitoring. Power is also supplied to the Data Acquisition Command Unit either through the Transmitter or directly in actual operation during the shot.

During the Operate, or Power Down and UP modes of the Command Transmitter the supply is programmed for a constant 50 Vdc. In the Charge mode the supply front panel voltage control knob is enabled for a 0 to 120 Vdc setting. When directly plugged into the DACU the supply is only programmed for 50 Vdc by a 15-kilohm resistor. The interconnect cable is terminated by a Bendix PT06A-16-11S(SR) 11-pin connector. Connections are as follows:

POWER SUPPLY TERMINAL	WIRE COLOR	CONNECTOR PIN
+(Power)	Red (#18)	C
-(Power)	Grey (#18)	J
A9 & +S	Orange (#22)	K
A5 & A6	Green (#22)	L
A7	Yellow (#22)	H

The following additional terminals of the supply should be connected: A1 to A2, -S to A8. (A3 and A4 are NOT connected.) During remote 50 Vdc programming a 15 kilohm resistor is switched between A9, +S and A5, A6. For manual control A7 is shorted to A5, A6 (see Figure 2.6-3).

The Underground Telemetry Rack Power Unit (Model 105841) contains two R/O Model 105 5 Vdc, 5 A power supplies. The input is 115 V, 60 Hz which is switched at the front panel. Also, at the front panel, jacks are provided to test the supply voltages. Power may be taken from these points if required. The supply is used to power analog, digital and display circuits in the Underground Telemetry Command Transmitter and Underground Telemetry Receiver. Interconnections to the receiver and transmitter are made through a fanned cable by a 19-pin connector, Bendix PT02A14-19S. Pin assignments are as follows:

POWER SUPPLY CONNECTION	USE	OUTPUT A (Long)	OUTPUT B (Short)
A	-5 V	A	NC
B	-5 V	B	NC
C	-5 V	NC	A
P	-5 V	NC	B
E	+5 V	C	NC
F	+5 V	NC	C
H	Return	F	NC
J	Return	E	NC
K	Return	NC	F
L	Return	NC	E
R	NC	D	NC
S	NC	G	NC
T	NC	H	NC
N	NC	NC	D
U	NC	NC	G
V	NC	NC	H

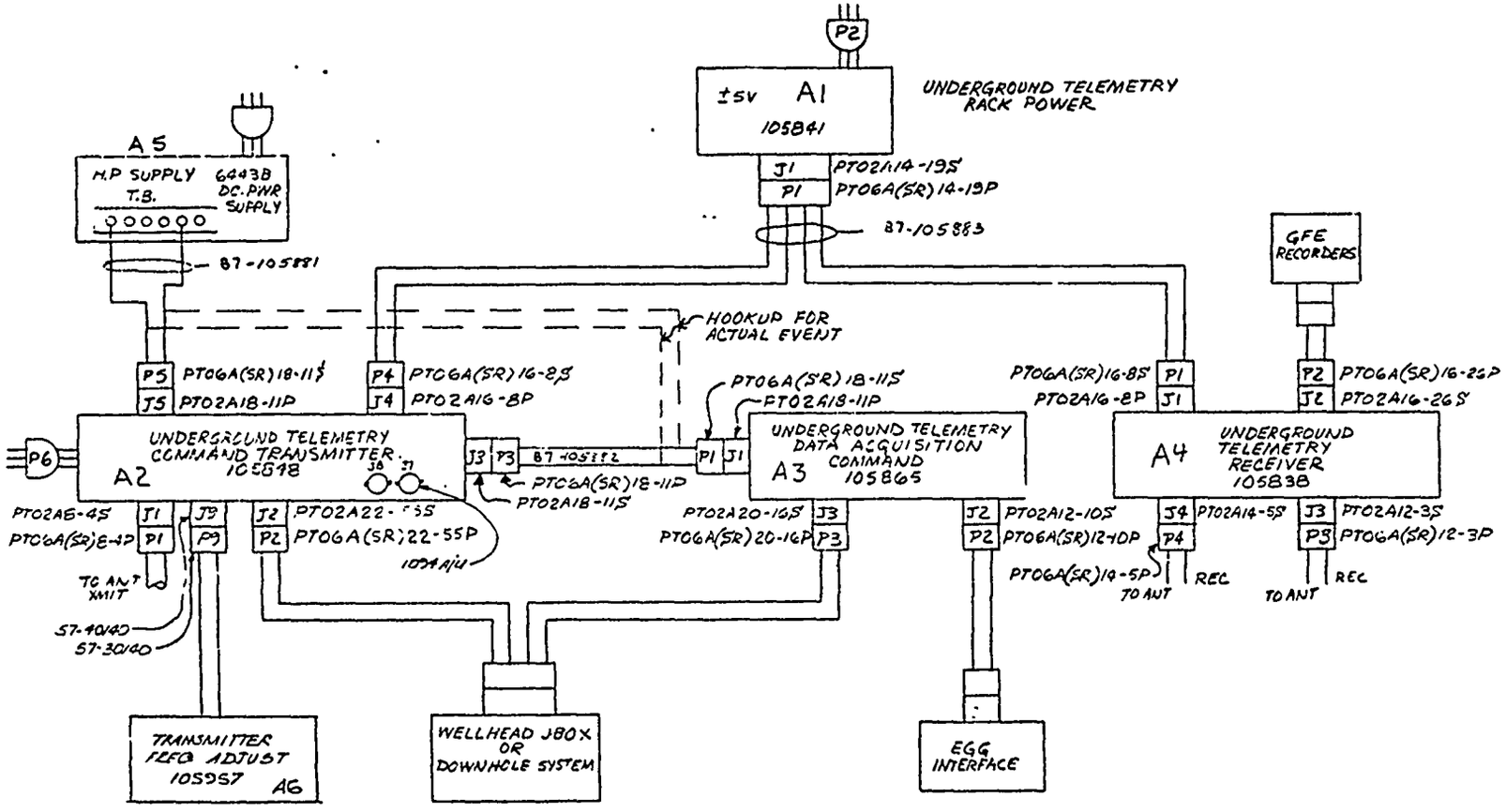


FIGURE 2.6-1

WELLHEAD INTERCONNECT DIAGRAM, 105470

2.6.2 Data Acquisition Command Unit Functions

To initialize the electronics and start the data acquiral mode in the downhole canisters, a Ready signal followed by a FIDU signal is required. These two signals come from the Wellhead System's Underground Telemetry Data Acquisition Command Unit (Model 105865) through hardwire cables to the downhole canisters.

The Data Acquisition Command Unit (DACU) and the HP Model 6443B power supply are the only two units required from the Wellhead System to initiate the data acquisition mode. The DACU contains one circuit card (Figure 2.6-2) which requires 50 volts dc for operation. Unit operation is automatic; however, it is provided with front panel manual test points to generate the required two 50-V dc signals for test operations.

The DACU provides a 50-volt output and receives a sustained 50 volt dc Ready level from the dual relay closures at the EGG interface at least 10 seconds and no more than 25 seconds before data acquisition is to begin. This signal is transmitted to each of the canisters through individual 51-ohm resistors. The actual data acquisition signal (FIDU) received from the EGG Pulse Transformer interface is a 50 V dc, 500 ns pulse which is lengthened to a 50 V dc, 150 microsecond pulse that is hardwire transmitted to each canister through 51-ohm resistors. The manual controls may be sustained levels, but the actual signal to the canister(s) will be a 150 microsecond pulse. Both signals drive opto-isolator switches in the EMP section of the downhole canisters.

The DACU may be powered directly from the 0 to 120 V dc supply cable, in which case the DACU will remotely control the constant voltage to 50 V dc. However, it may also be powered from the Underground Telemetry Command Transmitter when the transmitter is in the Operate mode only. The transmitter will control the voltage to +50 V dc only. Power connections may be made by the cable with pin assignments as follows:

PIN	ASSIGNMENT
C	50 Vdc
J	Return
K	Remote Programming
L	Remote Programming

Signal inputs from the EGG interface are made with a 10-pin Bendix PT02A12-10S connector with pin assignments as follows:

PIN	ASSIGNMENT
A	Power Return
B	50 Vdc output
D	FIDU input
F	Ready input
G	Shield

Command output connections are made to the downhole system via the Wellhead J Box through a 16-pin Bendix PT02A20-16S connector with pin assignments as follows:

PIN	ASSIGNMENT
A	FIDU Can #1
B	FIDU Can #2
C	FIDU Can #3
D	FIDU Can #4
E	Ready Can #1
F	Ready Can #2
G	Ready Can #3
H	Ready Can #4
J	Return

Required mating connectors are Bendix types PT06A(SR)12-10P, PT06A(SR)20-16P, PT06A(SR)18-11S (on cable), respectively.

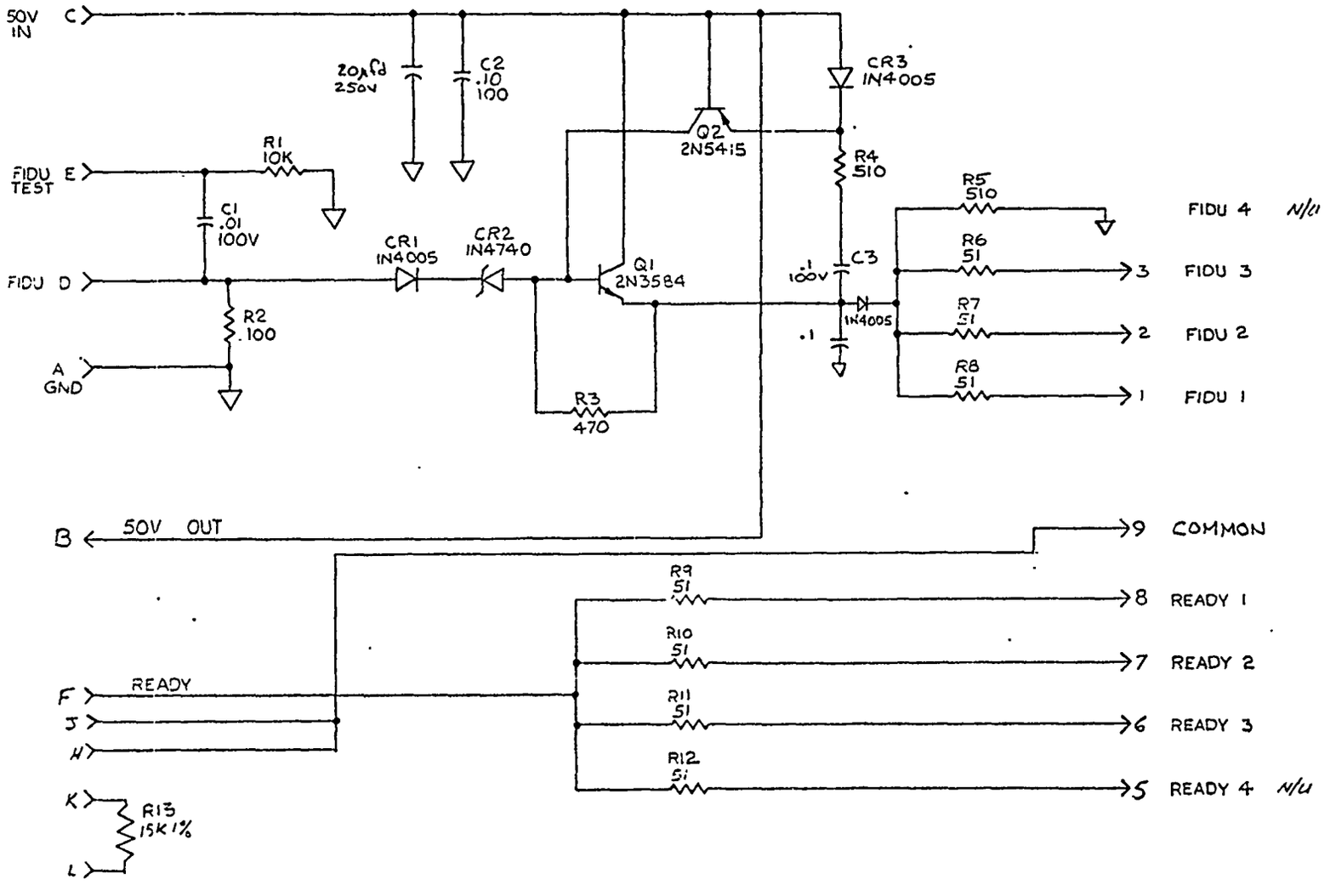


FIGURE 2.6-2

SCHEMATIC, FIDU/READY BOARD, DACU, 105884

2.6.3 Command Transmitter Unit Functions (Downlink)

The Underground Telemetry System Command Transmitter Unit (Model 105848) provides the following general functions

A. Hardwire power up commands, battery charging control and monitoring, and downhole transmit antenna monitoring for preshot operations.

B. Downlink RF transmission of an interrogate command word to the downhole canisters.

Table 2.6-1 describes the front panel controls and Table 2.6-2 describes rear panel connectors for the Command Transmitter.

2.6.3.1 Hardwire Functions

The following describes those functions of the Command Transmitter electronics which are used to initialize and monitor the downhole system, when the cable is still connected, shown in the schematic of Figure 2.6-3.

A Power Up Command is achieved by setting the POWER CONTROL Switch to the UP position, supplying +50 V dc to the COMMAND pushbuttons. Depressing the button(s) will cause power to latch up in the canister(s) selected by starting the standby inverter type regulator in the downhole unit. When power is on, the PWR MON Telemetry Link line(s) will pull approximately 750 microamperes through a transistor switch in the EMP filter section, causing the front panel LED's to turn on. The LED's are enabled in the OP and UP modes only. When the POWER CONTROL switch is in the DOWN position, -50 V dc is supplied to the COMMAND pushbuttons. Depressing the button(s) will cause a -50 V dc signal to turn all power off in the canister(s) by shutting down the standby regulator. By returning to the UP or OP mode, the state of the LED's indicate if power did in fact turn off.

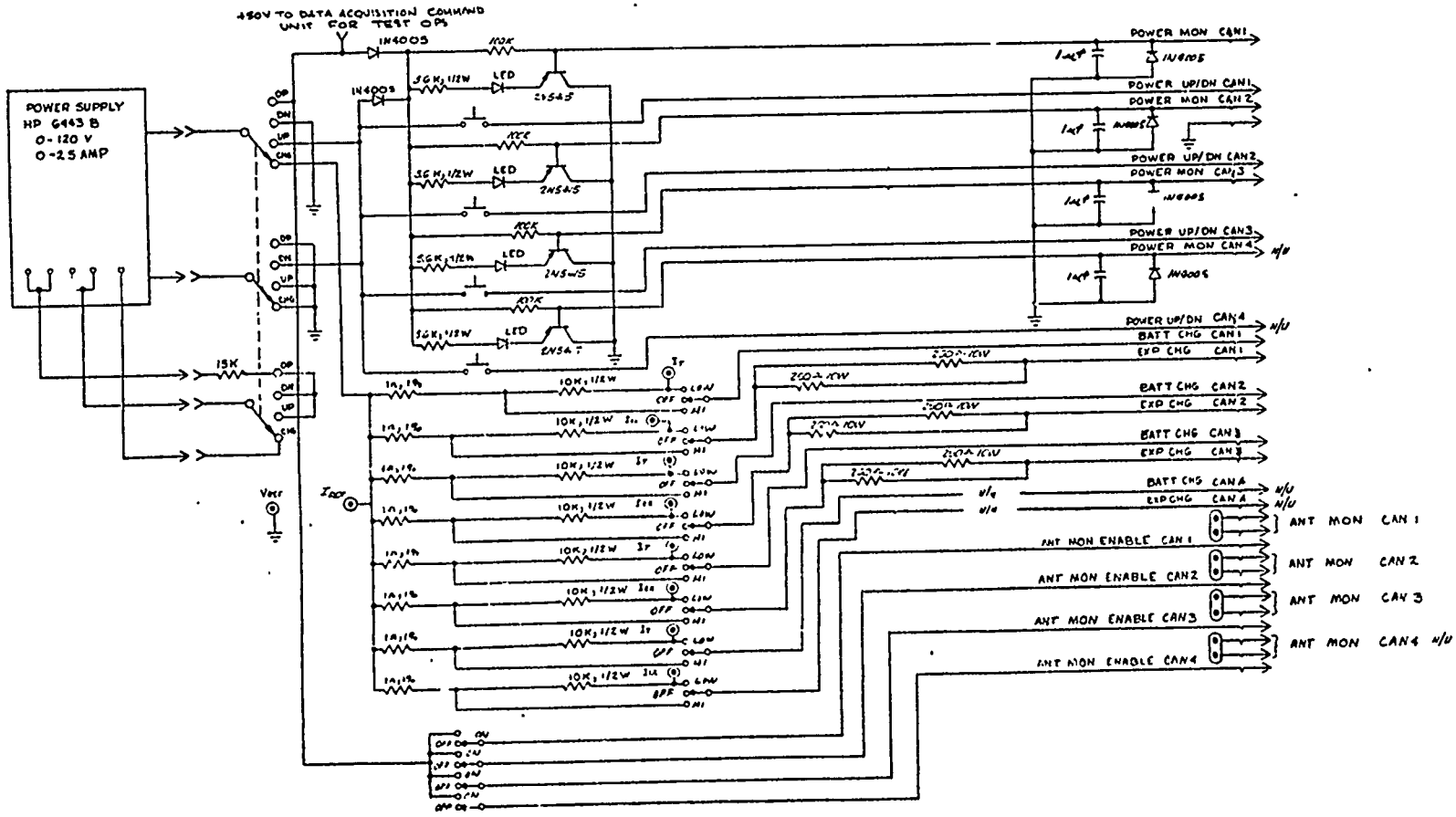


FIGURE 2.6-3

SCHEMATIC, COMMAND TRANSMITTER, 105848

The charge of each battery set is controlled by a 3-position switch (HI, OFF, and LOW). In the HI charge position the output for the TLM Battery is the HP supply setting (now controllable from the supply panel) in series with a 1 ohm monitor resistor. The output of the EXP charge is the HP supply in series with 250 ohms. The voltage read between the I_{REF} jack provided on the panel and the I_T or I_E jacks is proportional to the charge current by a proportion of 1 mV/mA. The voltage measured between V_{REF} and the I_T or I_E jacks is equal to the charge voltage on the downhole cable. The voltage is measured through a 10 kilohm impedance so the meter used should be at least 1 megohm input impedance to minimize the error. When the switch(es) are in the LOW charge position, 10 kilohm is added to the output impedance of each charge line. It is important that the power supply voltage be returned to zero after each activity. The details of battery charging requirements are given in Section 2.3 and 2.5.

The ANTENNA MONITOR switches are enabled in the OP mode only. The command output is a 50 V dc level when the switches are on, which biases a diode switch arrangement in the EMP section. The signal received back at the monitor jacks is an attenuated 1/2 wave rectified signal of approximately 500 mV pp from the downhole transmitter board output and will be imposed on a ≈4 V dc level.

TABLE 2.6 - 1

COMMAND TRANSMITTER

FRONT PANEL CONTROLS AND INDICATORS

The following lists the front panel controls and indicators and gives a description of their functions.

DESIGNATION	FUNCTION
INTERROGATE COMMAND	21 2-position toggle switches (up for a 1, down for a 0) which, along with the Data Rate, forms the Command Word transmitted to the canisters.
DATA RATE	5-position rotary switch which programs the 7-bit code which is part of the Command Word to instruct the rate at which the canister is to transmit data.
POWER UP/DOWN COMMAND	Momentary pushbutton which functions only in the UP or DOWN mode. Causes the canister to power up or down as selected.
TLM	
PWR	LED which is enabled only in UP or OP modes. When illuminated indicates power is on in canister.
Mode Control Switch	4-position rotary switch which controls the 0-120 V power supply programming and routes power for battery charging, antenna monitor, Power UP/DWN and the DACU. Does not control Interrogate Command transmission.
CHG	Only powers the battery charging circuits. The HP supply voltage control is functional.
UP	Only powers Power UP/DWN control circuit with 50 V dc for Power Up Command. Telemetry functional.
DOWN	Only powers Power UP/DWN control circuit with -50 V dc for Power Down Command. Telemetry not functional.
OP	Operate - supplies DACU with +50 V dc. Enables telemetry and antenna monitor system.
AMP POWER ON/OFF	2-position toggle switch controls 115V/60 Hz input power to Bogen 100 watt amplifier.
EXECUTE	White lighted pushbutton which causes transmission of the Command Word when armed. Light remains lit only during transmission.

ARM		Red lighted pushbutton which arms the command transmission (enables EXECUTE pushbutton). Lit when armed. Reset by pressing ARM again or pressing EXECUTE.
BATTERY CHARGE		Enabled in CHG Mode.
TLM		3-position, center off, toggle switch, one for each canister.
	HI	Maximum charge rate at 98 V dc for 72 V batteries.
	OFF	No charge.
	LOW	Battery Voltage Monitor Pos.
EXP		3-position, center off, toggles switches as above for TLM to charge 12 V batteries.
Charge Monitors		
TLM		Test Point to monitor charge current in HI charge rate mode. Voltage measured between this point and I_{REF} proportional to current by ratio 1 mV/mA.
EXP		Test Point as above tc monitor EXP batteries.
ANTENNA MONITOR ON/OFF		2-position toggle switch provides 50 V bias to antenna monitoring circuit downhole.
	Test Points	Antenna signal will appear between these points on approximately 4 V dc level.
I_{REF}		Common connection test point for monitoring I_T and I_E (This point = HP supply voltage in charge mode).
V_{REF}		Ground reference.

TABLE 2.6-2

REAR PANEL CONNECTORS

3-PIN POWER PLUG

115 V, 50-60 Hz
2.5 A

4-PIN ANTENNA SOCKET

A	Signal
B	Shield
C,D	NC

11-PIN DACU SOCKET (OP mode only)

C	+50 V (OP mode)
J	Return

11-PIN 0-120 V SUPPLY PLUG

C	0-120 V dc
J	Return
H	To A7 of HP Supply*
K	To A9 & S of HP Supply*
L	To A5 & A6 of HP Supply*

*Remote V Prog Pins

8-PIN ±5 V SUPPLY PLUG

A	-5 V dc
C	+5 V dc
F	Return

Remainder not connected

55-PIN J BOX SOCKET

A	Power UP/DWN Command, Can 1	T	TLM Charge Can 1
B	" Can 2	U	TLM Charge Can 2
C	" Can 3	V	TLM Charge Can 3
D	" Can 4	W	TLM Charge Can 4
E	Antenna Monitor, Can 1, Signal	X	Power U/DWN Telemetry Can 4
F	" Gnd	Y	" Can 3
G	" Common	Z	" Can 2
H	" Can 2, Signal	a	" Can 1
J	Gnd	b	EXP Charge Can 1
K	" Common	c	EXP Charge Can 2
L	" Can 3, Signal	d	EXP Charge Can 3
M	" Gnd	e	EXP Charge Can 4
N	" Common	HH	Return
P	" Can 4, Signal	EE	Return
R	" Gnd		
S	" Common		

2.6.3.2 Interrogate Command Function

A data dump from the downhole canisters is initiated by the Interrogate Command Transmitter shown in the block diagram of Figure 2.6-4. The Interrogate Command Word consists of 79 bits with the format shown in Table 2.6-3. Twenty-eight bits are programmable through the front panel. The electronics for the Interrogate Command Generator are contained on three PC boards as shown schematically in Figures 2.6-5, 2.6-6, and 2.6-7. The Command Word is transmitted in the form of a tristate FM (RZFSK) signal, amplified by a Bogen Model M0100A 100-watt amplifier at nominal frequencies of 79, 90 and 101 Hz. (The transmit antenna configuration and actual transmit power levels are discussed in Section 3.)

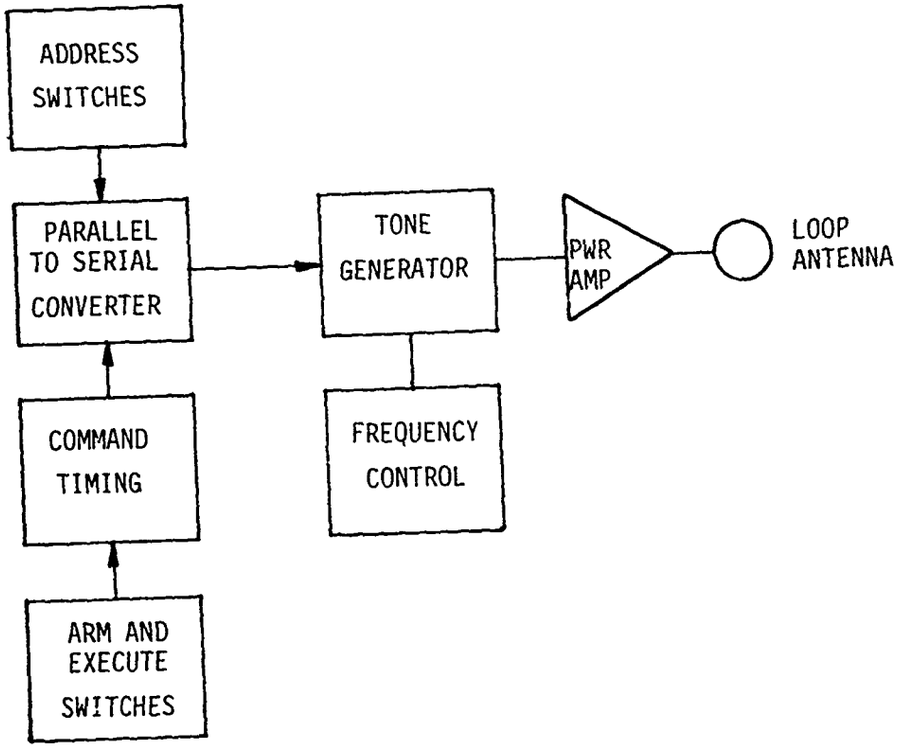


FIGURE 2.6-4

INTERROGATE COMMAND TRANSMITTER BLOCK DIAGRAM

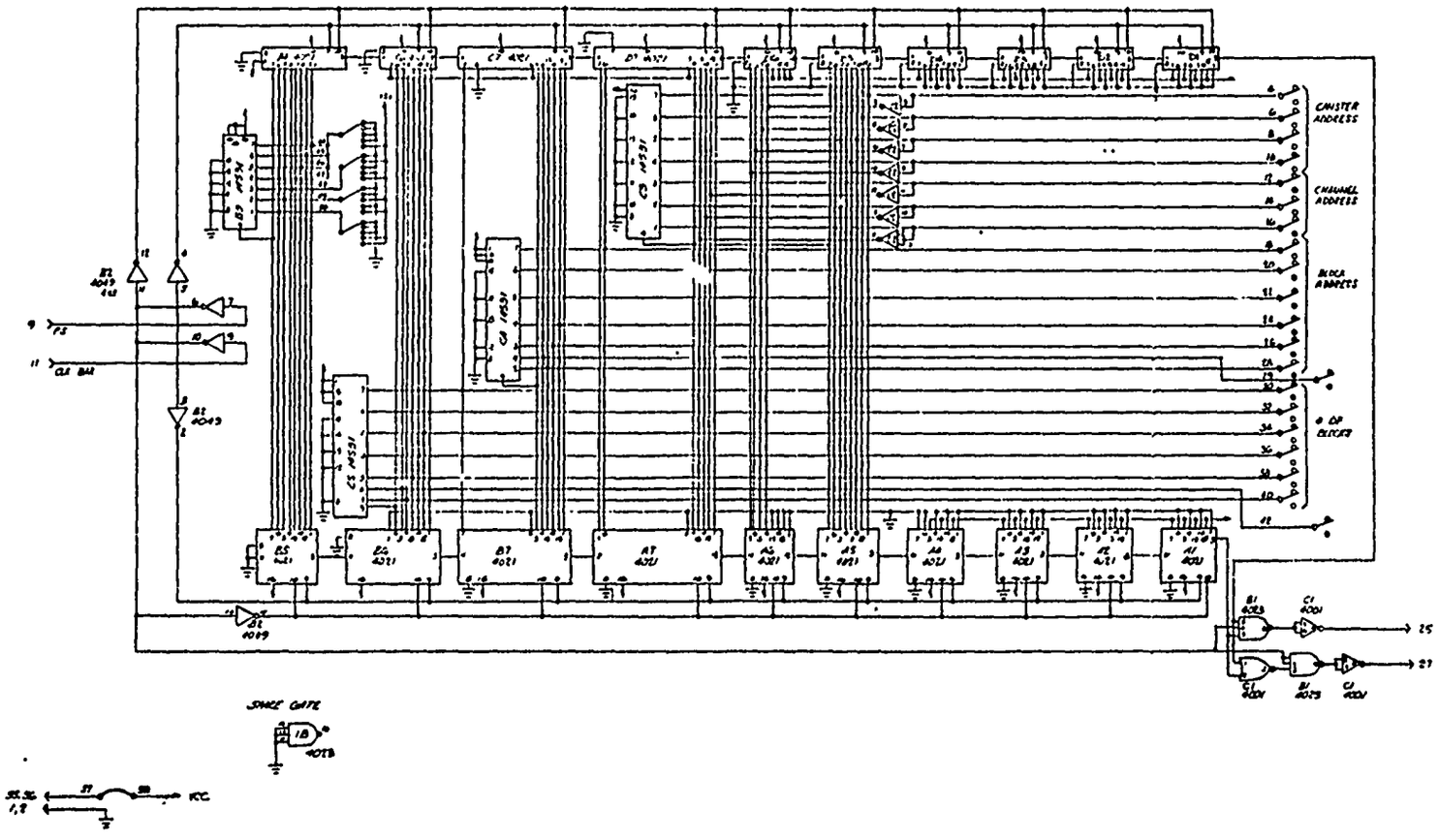
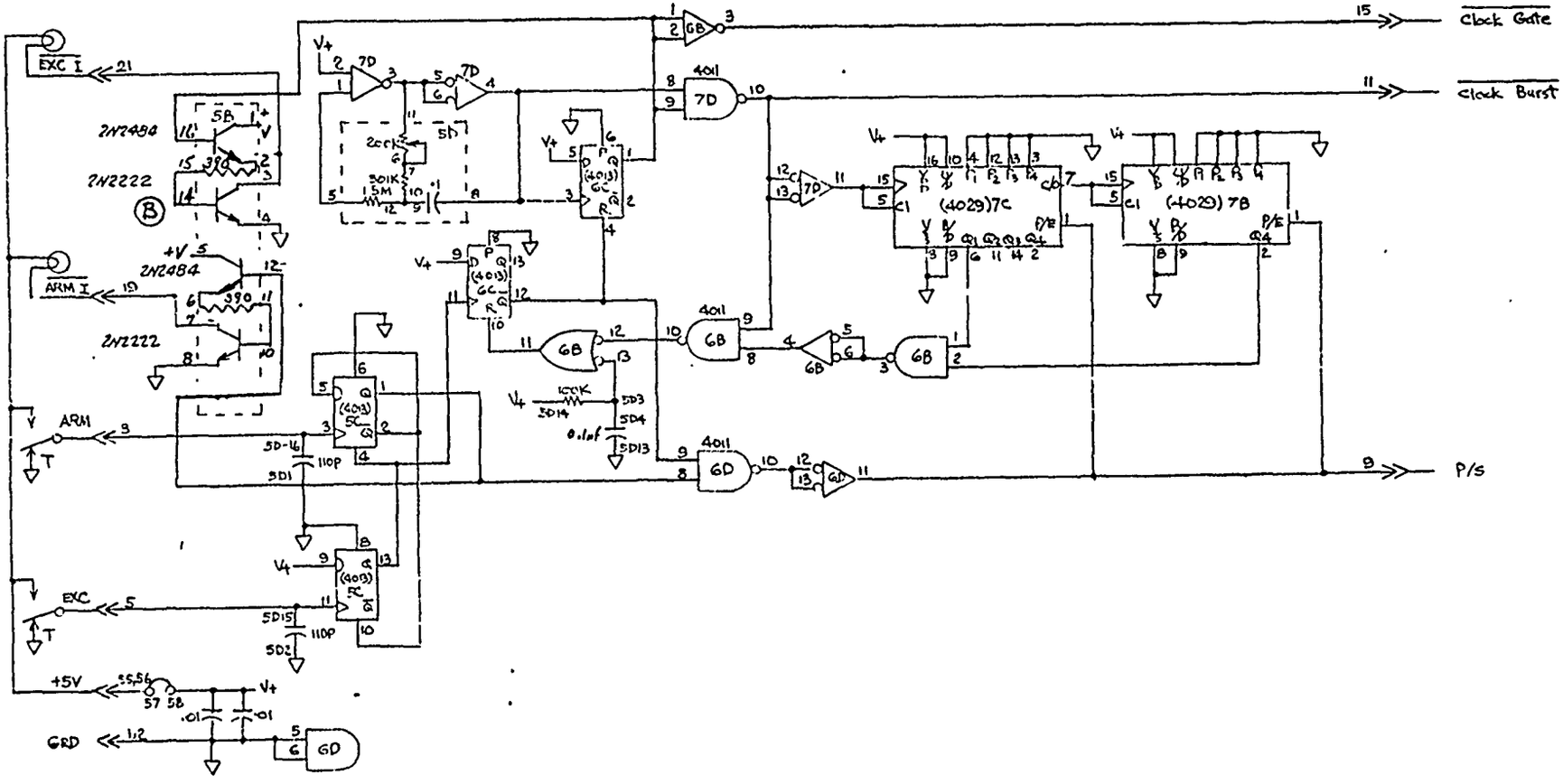


FIGURE 2.6-5

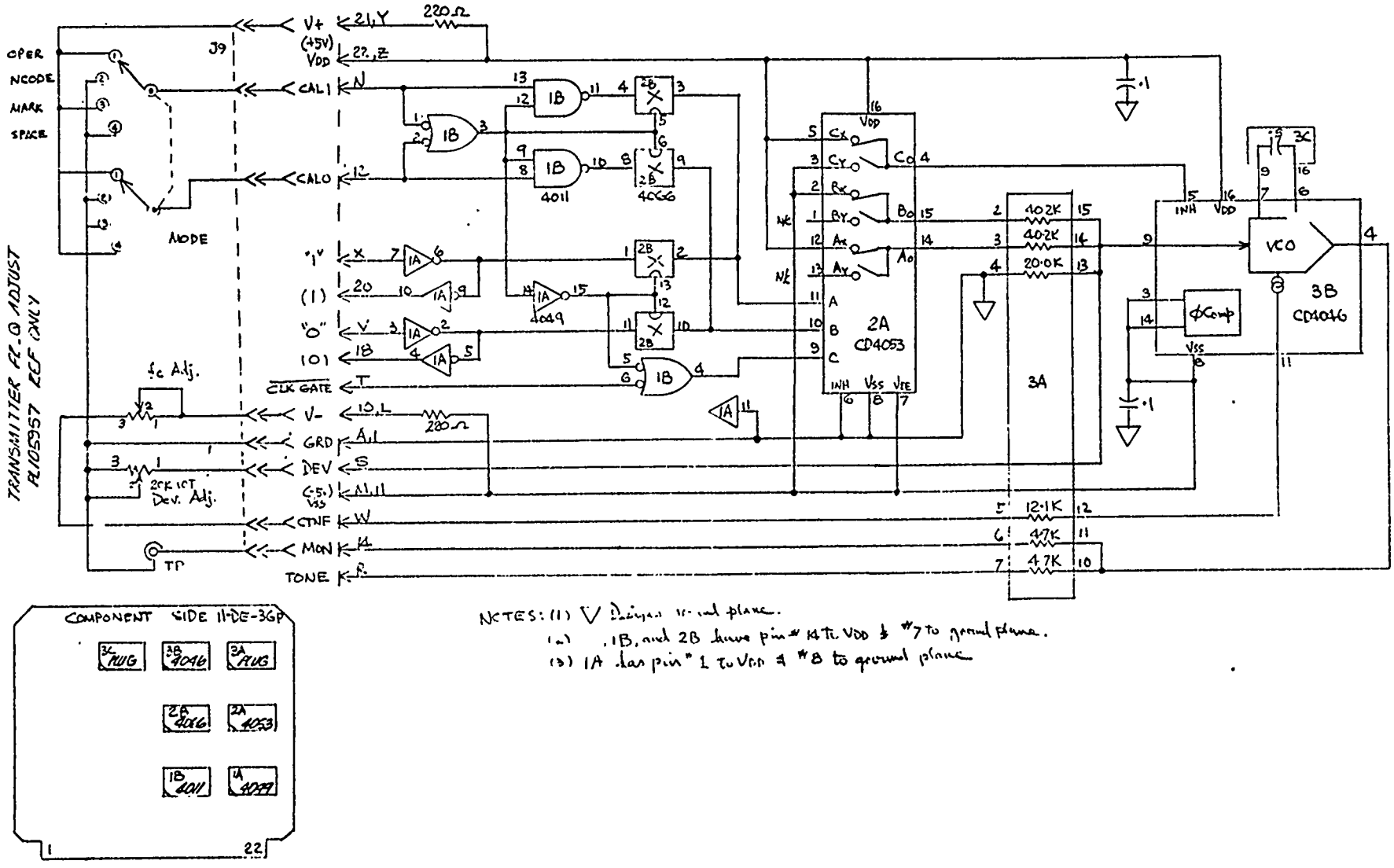
SCHEMATIC, INTERROGATE COMMAND PARALLEL-TO-SERIAL CONVERTER
105398



Notes: (1) IC 6B, 6D, 6C and 7D have pin #7 to GRD and #14 to V+

FIGURE 2.6-6

SCHEMATIC, INTERROGATE COMMAND TIMING, 105399



NOTES: (1) V Designates ground plane.
(2) 1B, and 2B have pin #14 to VDD & #7 to ground plane.
(3) 1A has pin #1 to VDD & #8 to ground plane

FIGURE 2.6-7

SCHEMATIC, TONE GENERATOR, 105864

TABLE 2.6-3

COMMAND WORD FORMAT

BITS	
1-31	Alternating 1's and 0's, starting and ending with 0
32	No code
33-36	Canister Address (MSB first)
37-39	Channel Address (MSB first)
40	Even parity bit for bits 33-39
41-43	No codes
44-47	$\overline{\text{Canister Address}}$ (MSB first)
48-50	$\overline{\text{Channel Address}}$ (MSB first)
51	Odd parity bit for bits 44-50
52	No code
53-59	Starting Block Address (MSB first)
60	Odd parity bit for bits 53-59
61	No code
62-68	Number of blocks fo data to be transferred (1 blk = 8 bytes)
69	Odd parity bit for bits 62-68
70	No code
71-77	Data Rate (see Table 2.6-4)
78	Odd parity for bits 71-77
79	No code (infinite time)

TABLE 2.6-4

DATA RATE CODE

BITS/SECOND	MSB						LSB
0.5	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0
2	0	1	0	0	0	0	0
4	0	0	1	0	0	0	0
128	0	0	0	0	0	0	0

The Command Word consists of a tristate code as formatted in the Parallel to Serial Converter Board, Figure 2.6-5. The two data lines are designated "1" and "0". Depending on which line is high, the bit is a 1 or a 0. If both lines are low, the bit is termed a no code. Note that for a 1 or a 0 bit a line must be high.

Transmission is initiated by depressing the ARM pushbutton on the front panel, which sets the D flip-flop in package 5C on the Interrogate Timing Board, Figure 2.6-6. This D flip-flop enables the second D flip-flop in the same package which may now be clocked by the EXECUTE pushbutton. If the ARM is set (as indicated by the lighted pushbutton) it may be reset by again depressing the ARM switch. When ARM is on, the parallel/serial control line to the parallel-to-serial converter board is high for parallel loading of the Command Word from the front panel into the shift registers on the converter board. Simultaneously the 4029 counters (7B and 7C) are set to zero. When the EXECUTE D flip-flop has been clocked high, a D flip-flop in 6C is set and the D flip-flops in 5C are reset in a ripple sequence. The 4029 Preset Enable and parallel/serial control lines are lowered. The second flip-flop in 6C will be set on the next positive edge of the oscillator, syncing the system with the clock. The Interrogate Command Timing Board will provide clock pulses to the Parallel/Serial Converter Boards until the 4029 counters have counted 79 pulses. During this period, the Clock gate line will be low and the EXECUTE switch will be lighted. When the counter reaches 79, the 2 flip-flops in 6C are reset in a ripple sequence and the circuit is ready for another operation. When data is entered into the 4021 shift registers of the Parallel/Serial Converter Board, it is entered in two identical sets of shift registers along with the preamble, no codes, and parity bits. During the serial shift of data, if the serial output of both sets of data are the same, the appropriate bit line will be high. If different, both will be low, causing a no code.

The function of the Tone Generator Board, Figure 2.6-7, is to generate the carrier tone for the interrogate command for downlink telemetry. There is a 1-7/8 inch front panel (Transmitter Frequency Adjust) associated with this board connected to the Command Transmitter Unit by a back panel mounted connector. A four-position rotary switch on the front panel determines the mode of operation for the tone generator. With this switch in the OP position, the tone generator will assume normal operation; that is, the tone generator will function as an FSK generator modulated by the interrogate command. When the switch is set at the other three positions, normal operation ceases, and the tone generator will

send out discrete tones according to the select positions for calibration purposes. The frequency of the generated tone can be measured at the front panel mounted BNC. One of the two 10-turn potentiometers sets the center frequency of the tone generator, NO CODE, while the other one controls the percentage of frequency deviation, MARK and SPACE.

The tone generator is implemented by the voltage controlled oscillator section within the CD4046 (3B). The center frequency of this VCO is determined by the 0.5 μF capacitor across 3B-6 and 3B-7, and the ten-turn 50 kilohm potentiometer labeled f_c Adj on the Transmitter Frequency Adjust front panel. Frequency modulation is accomplished by driving the VCO input (3B-9) with a resistor voltage summing network, where one of the resistor network elements is the 20 kilohm 10-turn potentiometer for frequency deviation adjust (DEV ADJ) on the Transmitter Frequency Adjust front panel. When the MODE switch is set at OP position, gate 1B3 will have both its input high and its output will enable transmission gates 2B-13 and 2B-12 via inverter 1A15. The incoming "ONE" and "ZERO" lines are inverted by 1A-6 and 1A-2, respectively, then fed to the "A" and "B" input of 2A. If the "ONE" line is high, one of the 40.2 kilohm resistors in the summing network will be connected to the 5-volt line; and if the "ZERO" line is high, the other 40.2 kilohm resistor will be connected to the -5 V line. The VCO will generate the desired frequencies only if its INH line is released. Section C of 2A works as a voltage translator of 1B4 which OR's the INH release gate. When the MODE switch is in any other position, other than the OP position, gate 1B3 will disable transmission gates 2B13 and 2B12; enable 2B5 and 2B6, and gate 1B4 which in turn enables the VCO. If the switch is set at NCODE position, both A and B sections of 2A will be activated, giving a net voltage of zero volts to the VCO. When the switch is set at MARK, only Section A is turned on, giving a positive voltage to the VCO. Similarly, the VCO will see a negative voltage when the switch is in the SPACE position. The magnitude of the control voltage is determined by the 50 kilohms potentiometer f_c ADJ on the Transmitter Frequency Adjust front panel. Two more inverters of 1A are used to buffer the "ONE" and "ZERO" lines for back panel monitoring purposes.

It is important to note that the downhole telemetry system must be initialized by going through a data acquisition cycle prior to interrogation. Once this is done, an interrogation may be accomplished by turning on the power amplifier with the front panel switch (allow tube warmup time before transmitting) and setting the 4 canister and 3 channel address switches as desired; the 7-bit number-of-block switches to the number of blocks of data to be transmitted from the canister (a block represents 8 bytes or 64 bits of information); and the data rate rotary switch to the rate at which data is to be transmitted from the canister. The ARM pushbutton will light when activated and indicate the command data is ready for transmission. Data contained in the switches has not been latched at this point and any change in the Command Word will be transmitted. The transmission may be disarmed by depressing the ARM button (push-on/push-off circuitry). If the EXECUTE button is depressed when the ARM light is on, transmission will take place. Any change in the Command Word will not be effective during EXECUTE and transmission is not abortable during EXECUTE. The transmitted Command Code may be monitored at the two BNC connectors on the rear panel. The outputs are 0-5 V dc digital signals. A five-volt level from the "1" output indicates 1 and from the "0" output indicates 0. If both signals are low, the bit is a no code.

2.6.4 Command Receiver Function (Downlink)

The RF transmission of the interrogate command word to the downhole canisters is sent from the Command Transmitter of the wellhead system. This RF signal is received at the canister by the Command Receiver board. The demodulated data from this board goes to the Command Receiver Decoder boards described in Section 2.2. They verify that the correct preamble, canister address, and MPU address have been received. If the command is valid, the MPU accepts the rest of the command data, which calls out the bit rate, first data block to be transmitted and number of data blocks to be transmitted.

The Command Receiver of the downhole system, Figure 2.6-8, consists of a high gain, limiting amplifier with a phase-lock FM detector at a center frequency of 90 Hz. A 60-Hz notch filter provides about 30 to 35 dB of attenuation to eliminate power line interference. Signals from the antenna are applied to a combination preamplifier/TR switch comprised of U1, U2, and Q2. Current feedback is employed through Q2 to the preamplifier input. TR switching is accomplished by diodes CR1, CR2, and CR3 which permit the preamplifier to withstand the full antenna voltage (75 V peak) during transmit mode.

The preamplifier output is applied to a limiter stage (U3) through a resistive network R14 and R15. 60-Hz notch filtering is achieved at the junction of R14 and R15. U6 and U7 form a gyrator which transforms C9 into an equivalent inductance which is resonant with C7 at the 60-Hz power line frequency. Thus, signal currents in R14 are shunted to signal ground. The limited output of U3 is applied to an active bandpass filter, U4, which has a 90-Hz center frequency and a 3-dB bandwidth of approximately 16 Hz. A second limiter and wave shaper (U5) follows the bandpass filter, U4. U5 has a small amount of positive feedback through C19 to provide a sharp leading edge trigger to the phase lock detector U8.

U8 is a CD4046 CMOS phase lock loop FM detector with a 90-Hz center frequency. C15 with R35 and R36 determine the VCO center frequency and range. The network containing R37, R38, R39, R52 and C16, C17, C18 and C20 provides the loop output filtering. The demodulated output from the phase

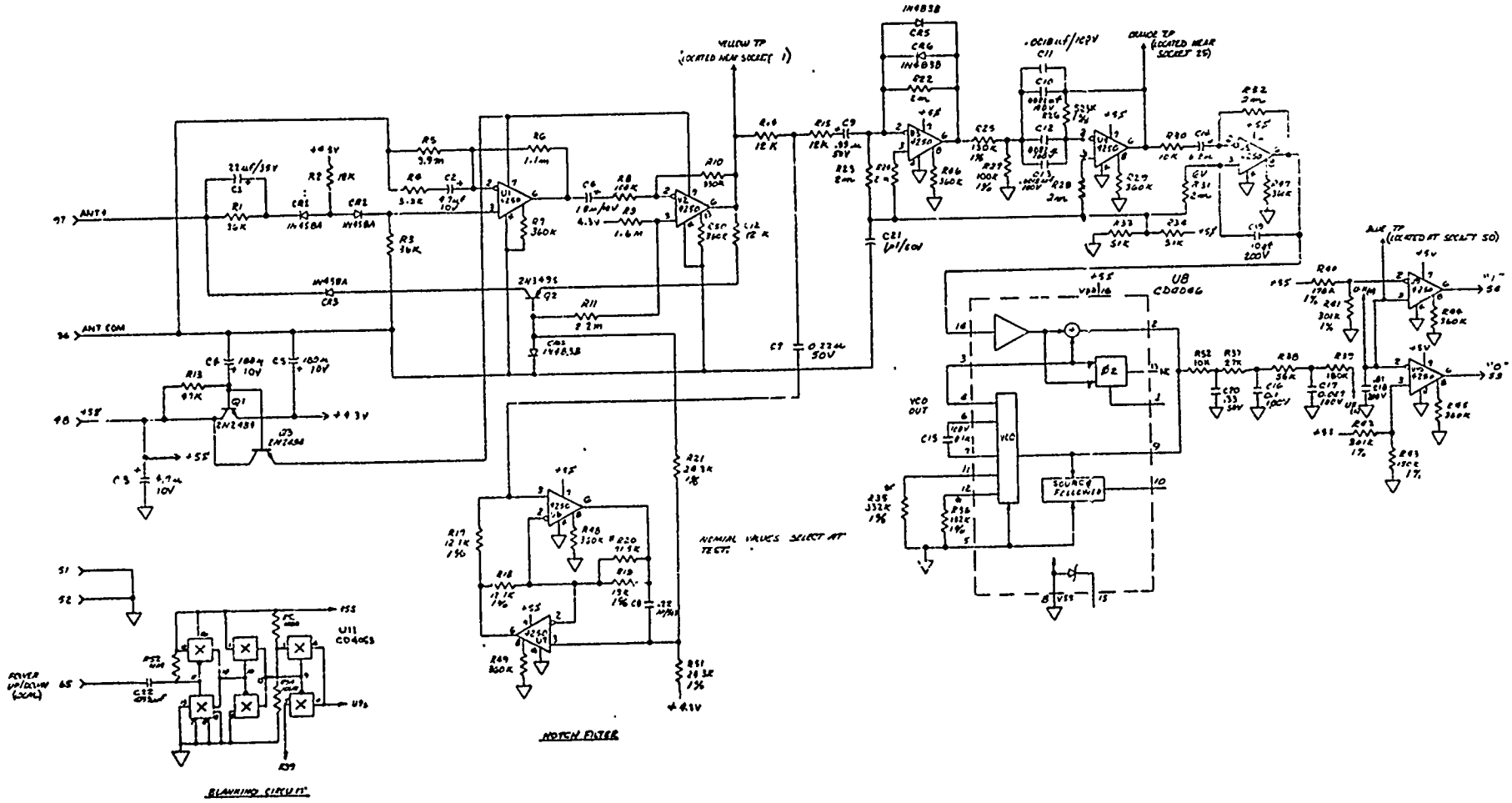


FIGURE 2.6-8

SCHEMATIC, COMMAND RECEIVER, 105497

locked loop is applied to threshold comparators U9 and U10, which provide the "two-wire" demodulated logic output levels. To eliminate the effects of transients caused when the MPU is powered up, U11, an analog multiplexer used as a gate, was added to provide approximately 15 milliseconds of blanking (determined by C22) during the no code time this switching occurs.

2.6.5 Underground Telemetry Transmitter Function (Uplink)

Once the interrogate command word, described in Section 2.6.3 is verified by the Command Receiver Decoder in the downhole system, the MPU will turn on, as discussed in Section 2.2, and transmit a serial digital mark/space code to the transmitter which supplies an FSK signal to the antenna at nominal frequencies of 84 and 80 Hz. The RF transmission of the downhole data is received at the wellhead by the Underground Telemetry Receiver, described in Section 2.6.6, where it is discriminated, decoded, and formatted for display and recording.

The Transmitter circuit, Figure 2.6-9, is a self-excited 84-Hz oscillator which uses the antenna and antenna-tuning capacitors as the frequency determining elements. The operating efficiency is approximately 90%. The actual oscillator is comprised of transistors Q1, Q2, and Q3 with positive feedback necessary for sustaining oscillation provided by transformers T1 and T2. Q4 supplies base current to Q3 and acts as a transmit enable command. FSK modulation is achieved in the circuit containing Q5, U1, U2, Q6, and triac Q7, an RCA 40526. The function of the modulator is to switch the capacitor bank comprised of C4 through C19 in or out of the resonant antenna circuit in accordance with the state of the data input line (Pin 89). Switching is done only on zero voltage crossings as detected by Q5 to ensure spurious-free modulation.

The transmitting antenna is a magnetic dipole consisting of an iron cored solenoid as described in Section 4.2.4. The core consists of 105 ±5 lbs (47.6 kg ±2.3 kg) of 0.006 inch (0.15 mm) thick Alleghany Ludlum #4750 laminate material with a net volume of 1.468" x 2" x 120" (3.73 cm x 5.08 cm x 304.8 cm). The winding consists of nominally 164 turns of four parallel strands of #10 AWG copper magnet wire wound over approximately 116 inches (294.6 cm) of the core length. The antenna inductance may be defined in terms of an effective area and an effective length[5]

$$L = \mu_0 N^2 \frac{A_e}{\ell_e}$$

where N is the number of turns. In this case, the effective length is the mean of the winding length and the core length or

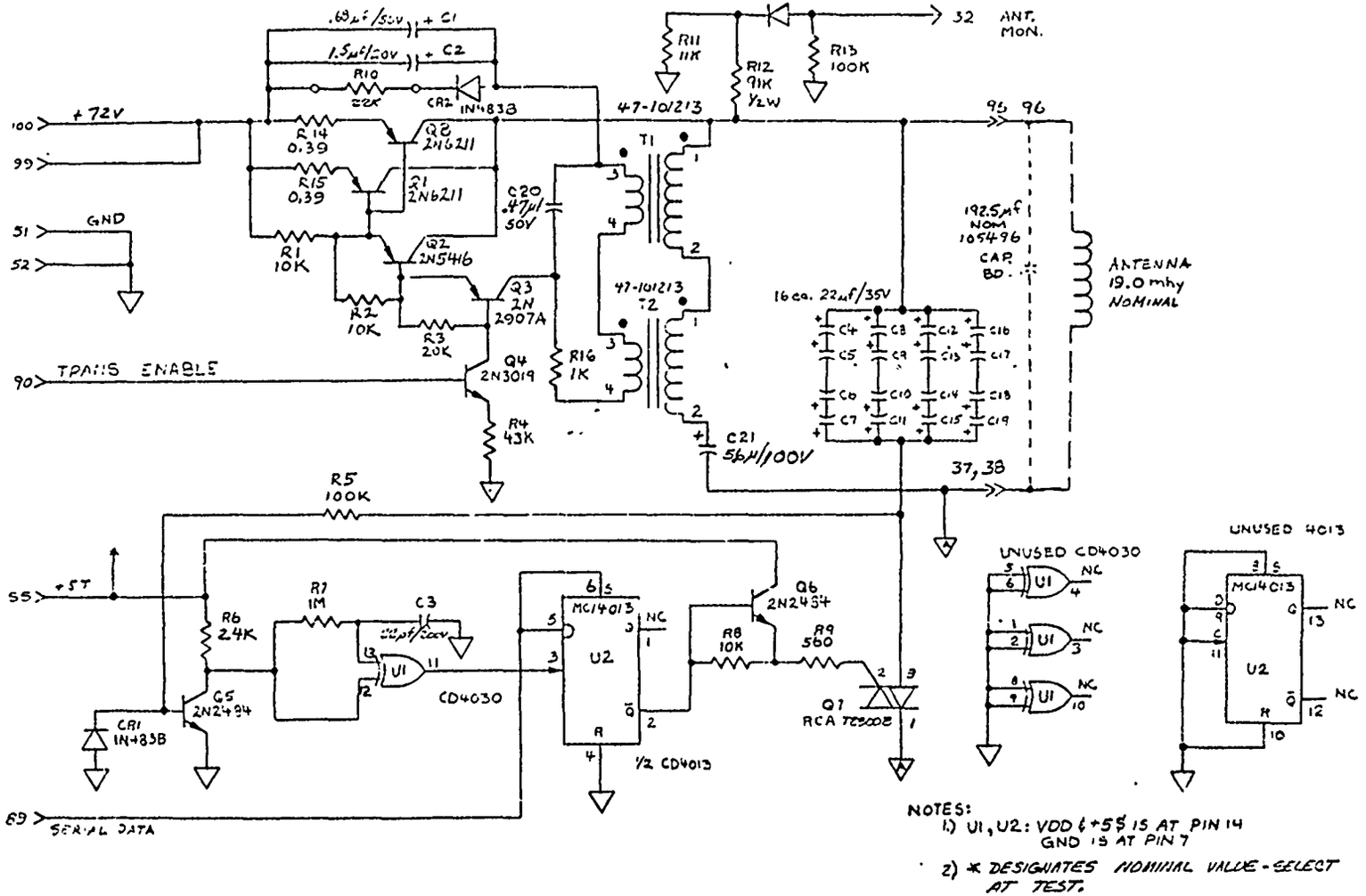


FIGURE 2.6-9

SCHEMATIC, S&F TRANSMITTER, 105472

$$\ell_e = \tfrac{1}{2} (\ell_w + \ell_e).$$

The core permeability and dimensions are such that the antenna is called geometrically limited. That is, the antenna permeance is purely a function of the dimensions (up to some limit) and does not significantly increase with an increase in core permeability. The effective antenna volume, S, in this case is given by the approximate expression

$$S = \frac{2\pi a^3}{\ell n(\frac{2a}{b}) - 1} = A_e \ell_e$$

where a is the core half length and b is the equivalent radius of the core. The calculated antenna inductance is therefore on the order of 21 mH but the measured values ranged from 18 to 19 mH due to manufacturing variations (e.g., number of turns) and systematic measuring errors such as detuning effects in the lab, etc.

The mark frequency is determined by the resonance of the separate capacitance boards and the antenna or

$$f_m = \frac{1}{2\pi \sqrt{C_m L}} .$$

Since the antenna inductance is fixed, the nominal 192.5 μF value of C_m ranged from 194 to 196 μF, resulting in mark frequencies ranging from 82.6 to 84.8 Hz, as measured in the lab, and 84 to 86 Hz, as measured in the field, which was well within the receiver limits.

The space frequency is achieved by switching the onboard capacitors (C4 to C19) in parallel with C_m by turning the triac (Q7) on, so that

$$f_s = \frac{1}{2\sqrt{(C_A + C_S)L}} = f_m \left(\frac{C_A}{C_A + C_S}\right)^{\frac{1}{2}}$$

Since the nominal value of C_S is about 22 μF, this results in a space frequency approximately 4 Hz lower than f_m. In practice, f_s ranged from 78.7 to 79.4 Hz in the lab and 80 to 82 Hz in the field — again, the variations are well within the receiver limits.

The fields produced by the transmitting antenna (see Section 3) may be determined from the magnetic dipole moment[5]

$$m = A_e N I$$

which may also be expressed as

$$m = \left(\frac{P_T S}{\Omega \mu_0}\right)^{1/2}$$

where I is the antenna driving current, P_T is the antenna input power, Ω is the angular antenna bandwidth, and A_e and S are the effective area and effective volume discussed above.

The antenna power can be calculated from[7]

$$Q = \frac{2\pi f(\text{Stored energy})}{\text{average power loss}} = \frac{\omega_0(\frac{1}{2}C V_p^2)}{P_T} = \frac{\omega_0(\frac{1}{2}L I_p^2)}{P_T}$$

and

$$P_T = \frac{1}{2}R I_p^2 = \frac{V_p^2}{R}$$

where R is the antenna input resistance due to core and coil loss, etc. The peak voltage, V_p, is essentially the battery voltage less some drop in the oscillator circuit, or about 72 volts. For average values of C = 195 μF, L = 18.6 mH, Q = 19, and f = 82 Hz, the antenna input power is approximately 14 watts and the antenna moment is approximately 1500 A-T•m^2. Note that this is significantly below the core saturation limit of 4600 A-T•m^2 and was chosen because of available energy constraints.

2.6.6 Underground Telemetry Receiver Unit Function (Uplink)

The functions of the Underground Telemetry Receiver (Model 105838) are to amplify and filter the signal received by the antenna, to coherent detect and decode the incoming signal, to process and display the content of the incoming signal, and to serve as test equipment during the fabrication and installation of the uplink transmitter. Figure 2.6-10 is the block diagram of the uplink receiver, and Table 2.6-5 is the functional description of the front panel.

The uplink signal is picked up by a loop antenna and amplified by the preamplifier which has a typical gain of 80 dB. The amplified signal is then fed to the repeater preamplifier through Twinax cable. Within the repeater preamplifier, notch filters are inserted to reduce the 60-Hz harmonic pickup. The amplitude-limited output of the repeater preamplifier drives the uplink detector.

The input active frequency of the uplink detector is tunable by a front panel mounted potentiometer, while the center frequency of the phase lock loop discriminator is fixed. The discriminated signal and the carrier amplitude detect signal are fed to the timer and synchronizer and the control and decode boards via a toggle switch. This switch is used to select the signal source either from the radio link mentioned above or high level signals from electrical cables.

The timer and synchronizer coherently demodulate the incoming signal, and convert it to NRZ serial data by generating synthesized clocks and gates. Front panel mounted monitor points and manual override controls are included to synchronize data whenever low level telemetry signals or high noise prevent automatic synchronization. A simple D/A converter is included for quick look capability with a strip chart recorder but it is intended that the serial digital data be recorded on magnetic tape for final reduction by computer. The control and decode board processes and decodes the incoming data byte by synchronizing itself with the encoded byte synchronization bits. Manual maneuver of the incoming signal is also made possible by front panel mounted controls. Processed data is fed to the error and byte display board as well as the data display board. Data in analog form is also available at the front panel.

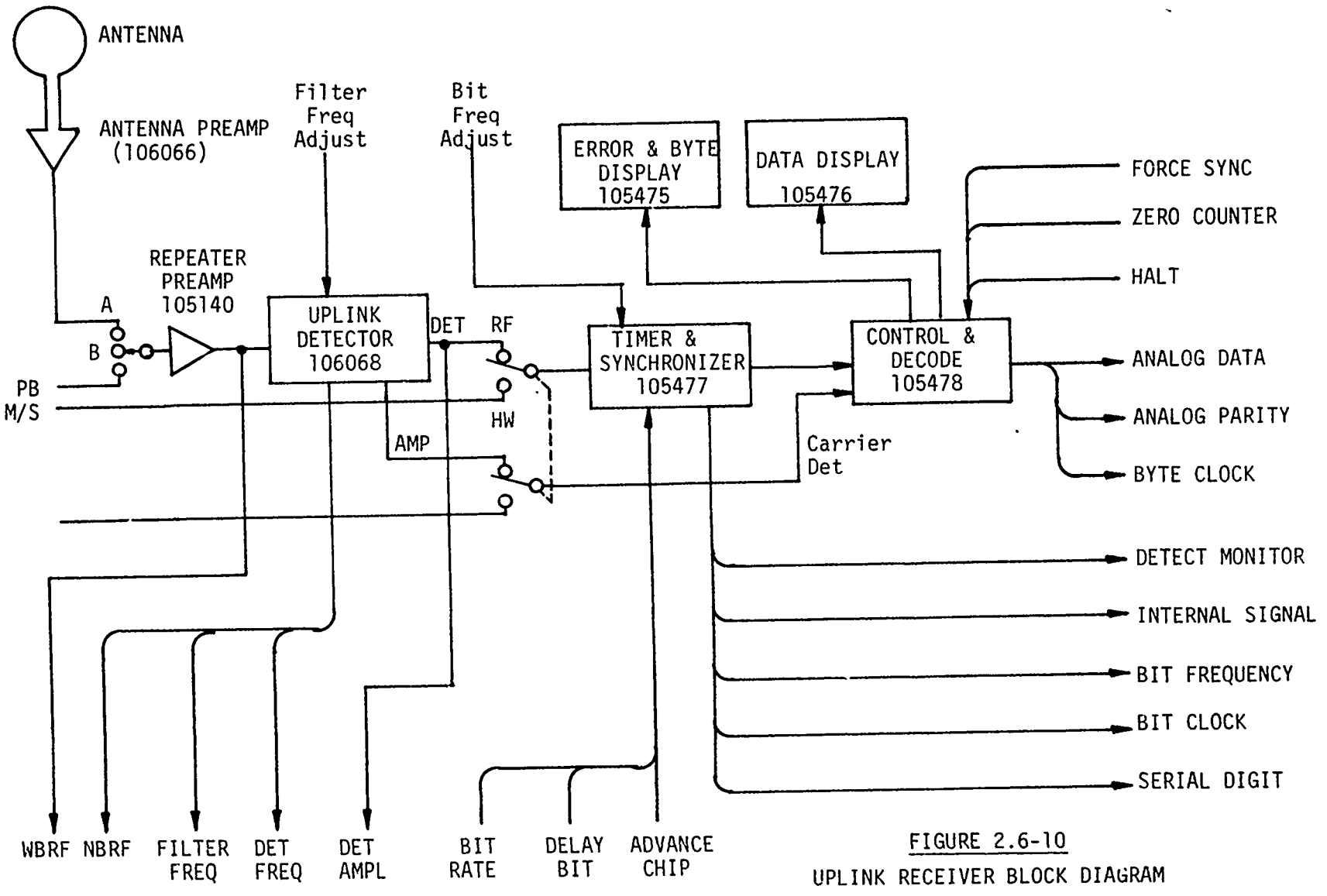


FIGURE 2.6-10

UPLINK RECEIVER BLOCK DIAGRAM

TABLE 2.6-5

UPLINK RECEIVER FRONT PANEL CONTROLS AND INDICATORS

CONTROL	DESCRIPTION
RECEIVER SOURCE SWITCH #1	Three-pole, 2-position switch to select signal source from hardwire or modulated signal source from radio link. When this switch is in the HW position, the enable gate and data will be coming in "T" and "M/S" BNC's, respectively. When this switch is in the RF position, signal can be coming from any one of the three sources selected by source switch #2.
RECEIVER SOURCE SWITCH #2	Three position rotary switch to select signal source from one of the following: Antenna A connector, Antenna B connector, or playback recorder BNC located at the back panel when source switch #1 is set at RF position.
FILTER FREQUENCY ADJUST	Ten-turn potentiometer to tune the frequency of the input bandpass filter of the uplink detector.
BIT FREQUENCY ADJUST	Ten-turn potentiometer to set the center frequency of the VCO located on the Timer and Synchronizer board to agree with the incoming data rate.
DECODER MODE SWITCH	Three-position toggle switch. In the center position, the decoder will function normally; that is, to acquire bit and byte sync. In the right momentary position, the decoder is inhibited from operation and all the data registers are cleared. In the left position, the decoder is allowed to be free running and process data regardless of synchronization.
BIT RATE SELECT	Five-position rotary switch to select integrator time constant for various data rates in conjunction with the BIT FREQ pot. Note that the "128" position is valid only during hardwire telemetry.
DELAY BIT	Momentary pushbutton to delay the byte clock by skipping one bit clock. The "DELAY" LED will turn on upon actuate and self-turn off after execution.
ADVANCE CHIP	Momentary pushbutton that will advance both the I and Q clock on the timer and synchronizer board 180° upon activation. Its function is used primarily to assist the synchronizer to acquire lock.

Table 2.6-5 continued.

ZERO COUNTER	Momentary pushbutton that resets both the parity errors and byte counters to zero.
FULL SCALE & ZERO CALIBRATION	Three-position momentary toggle switch used strictly for calibration purposes. Full scale and zero calibration is achieved by jamming 1's and 0's into the D/A registers. The BNC monitor is labeled "AN DATA".
GO and HALT	Three-position, center off momentary toggle switch used to override the normal parity errors and bytes counters functions. During normal operation, both the counters assume operation upon byte acquisition and terminate their activity upon loss of carrier; at the same time, the HALT indicator lights up.
CARRIER	LED indicator that indicates presence of carrier or enable gate during hardwire TM.
BIT	LED indicator that will turn on when the BIT DETECT circuitry recognizes seven 1's in a consecutive eight bits providing carrier detection is confirmed.
BYTE	LED indicator used for recognition of the byte code by its decoding circuitry. This LED will come on only if both carrier and bit have been recognized.
PARITY ERRORS	LED lamp used to indicate the detection of an erroneous parity bit.
DELAY	LED indicator that lights up upon actuation of the relay bit pushbutton and goes out upon execution.
HALT	LED indicator that signals the completion of each transmission or the actuation of its associated switch.
DATA DISPLAY	Three-decimal-digit display for each binary byte of data. Maximum value is 255.
PARITY ERROR COUNTER	Two-decimal-digit display used to register the number of parity errors during each transmission. Display resettable by ZERO COUNTER.
BYTES COUNTER	Three-decimal-digit display used to register number of data bytes during each transmission. Resettable by ZERO COUNTER.

Table 2.6-5 continued.

T BNC	BNC input to accept enable gate during hard-wire telemetry.
M/S BNC	BNC input to receive data line during hard-wire telemetry.
Spare BNC	BNC reserved for possible further modification.
NFRF BNC	Test point on repeater preamp board after input gain and notch filter stages but before clipping.
WBRF BNC	Test point to the input of the carrier band-pass filter on the uplink detector board (after clipping).
NBRF BNC	Test point for the output of the carrier band-pass filter on the uplink detector board.
FILTER FREQUENCY BNC	Test point for the square wave that is phase locked to the incoming carrier on the uplink detector board.
DETECTED FREQUENCY BNC	Test point for the discriminated incoming data by the phase lock loop on the uplink detector board.
DETECT AMPLITUDE BNC	Test point for the output of the carrier amplitude detector circuitry on the uplink detector board.
DETECT MONITOR BNC	Test point for the output of the input buffer on the timer and synchronizer board.
INTERNAL SIGNAL BNC	Test point to monitor the coherently detected incoming data on the timer & synchronizer board.
BIT FREQUENCY BNC	Monitor point for the loop stress voltage that drives the VCO on the timer & synchronizer board.
BIT CLOCK BNC	Output point of the synthesized clock which strobes in data. This clock is a buffered CLK B.
BYTE CLOCK BNC	Output point of the byte clock generated on the control and decode board by counting the synthesized CLK B after byte synch.
SERIAL DIGIT BNC	Output point of the detected NRZ data in serial form.

Table 2.6-5 continued.

ANALOG DATA BNC	Output point of the D/A converter that processes the incoming data byte on the control and decode board. Full scale and zero calibration switch located on the front panel.
ANALOG PARITY BNC	Test point that indicates an erroneous parity bit, when its level changes from -5 to +5 V.

2.6.6.1 Antenna Preamp (106066)

The antenna preamplifier, Figure 2.6-11, is constructed with an RCA CA3095 super-beta transistor array. It provides a typical gain of 80 dB to the signal referred to the input.

The signal picked up by the antenna is transformer-coupled to the first stage differential amplifier. The differential outputs of the first stage amplifier are coupled to the second stage by two 0.1 μF capacitors. The second differential amplifier has a current source output which is transformer-coupled to the mating cable by T2.

Battery and on/off switches are integrated to this preamp to avoid ground loop noise problems.

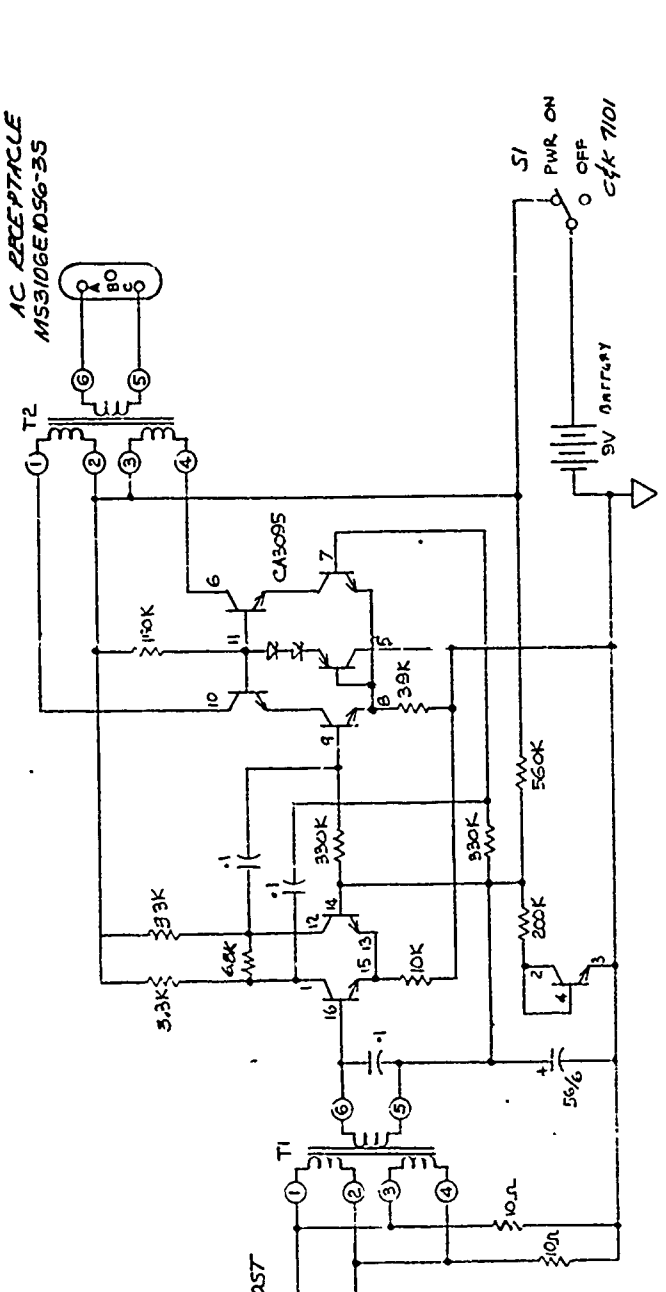


FIGURE 2.6-11

SCHEMATIC, ANTENNA PREAMP, 106066

2.6.6.2 Repeater Preamp

The repeater preamplifier, shown in the block diagram of Figure 2.6-12 and the schematic of Figure 2.6-13, provides signal conditioning and limiting for the uplink transmitted carrier. The incoming signal from the uplink antenna preamplifier is transformer coupled to the first stage bandpass filter implemented with one section of the 2144 triple op-amp device. This filter has its center frequency at 150 Hz with a gain of 18 dB. Q1 and Q2 (both 2N3965) are configured as an input differential amplifier for this stage mainly to keep the input equivalent noise low. The second bandpass filter has its center frequency at 65 Hz with a gain of 17 dB. Again, this stage is also implemented with a section of the 2144. Three notch filters are inserted between the first and the second bandpass filter. The 180-Hz and the 120-Hz notch filters are implemented with two LM4250 op-amps configured as a gyrator to simulate an inductor. The 60-Hz notch filter is implemented with two sections of 2144, and it can be switched in or out of the circuit by a back-panel mounted toggle switch. Frequency response (before limiting) with and without the notch filters is shown in Figure 2.6-14. Following the second bandpass filter are two limiter amplifiers, Each of the limiters are implemented with a section of the 2144, and diodes from U3 are used for output clamping. Transistors Q3 and Q4 serve as a capacitor multiplier for C1 and C7, respectively, to reduce noise pickup from the power rails.

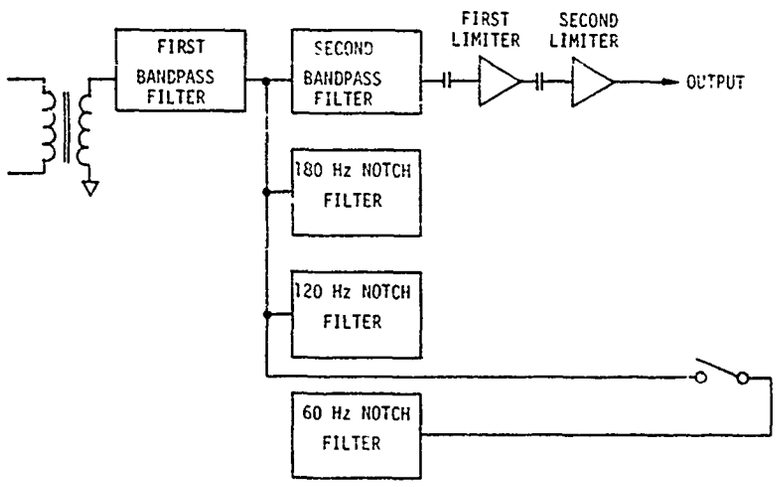


FIGURE 2.6-12
BLOCK DIAGRAM

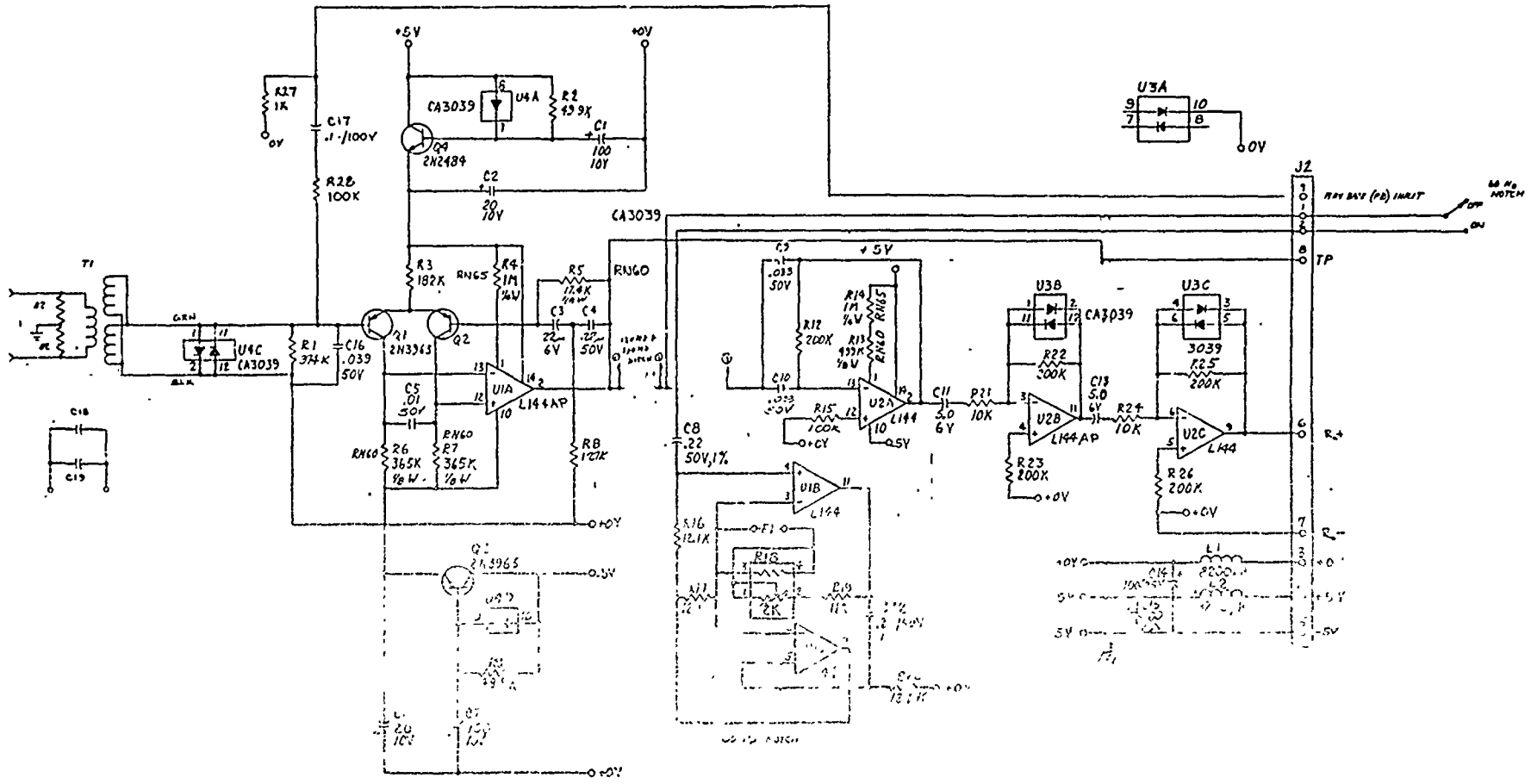


FIGURE 2.6-13A

SCHEMATIC, REPEATER PREAMPLIFIER, 106116

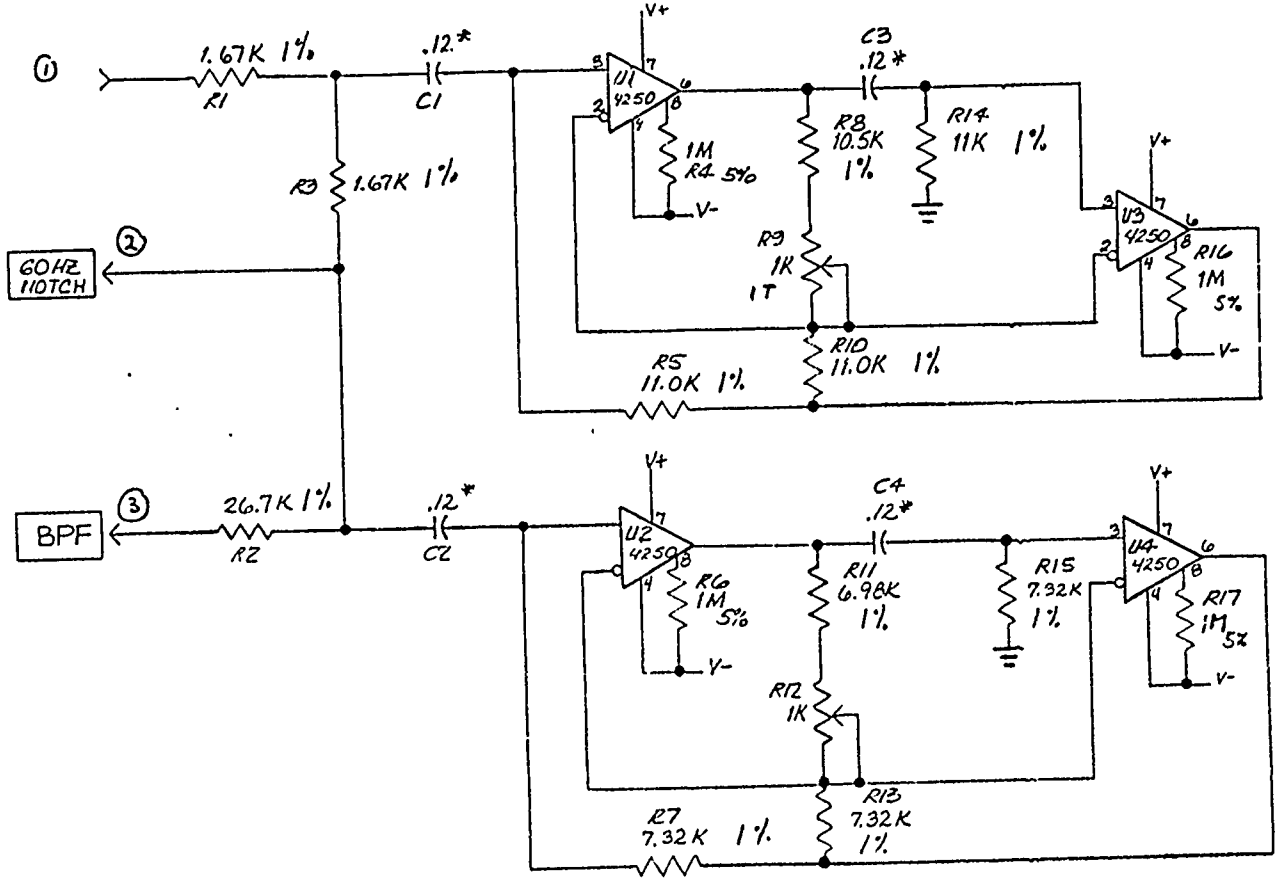


FIGURE 2.6-13B

SCHEMATIC, NOTCH FILTER, 106155

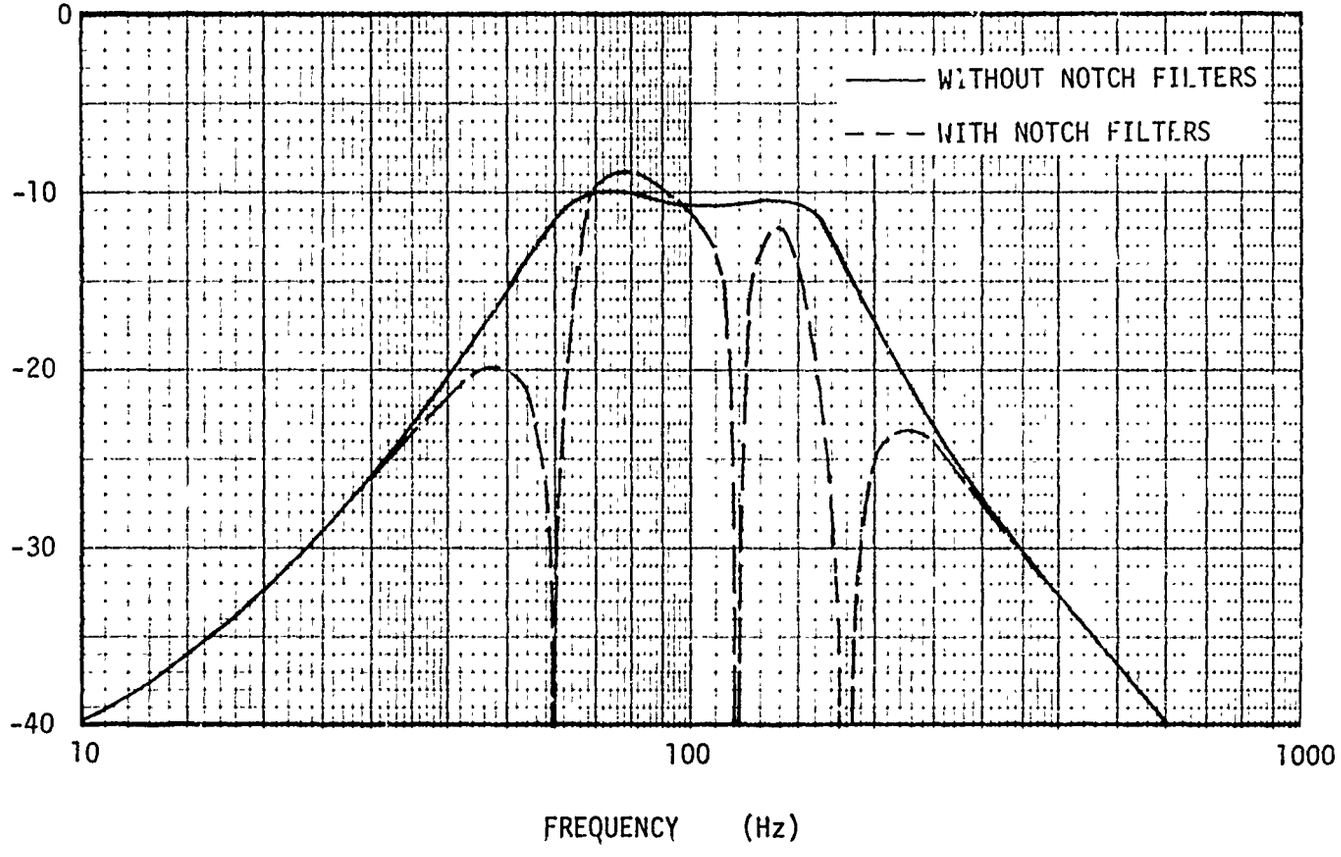


FIGURE 2.6-14

WELLHEAD REPEATER/PREAMP FREQUENCY RESPONSE

2.6.6.3 Uplink Detector - 106068

The purpose of the uplink detector, shown in the block diagram of Figure 2.6-15 and the schematic of Figure 2.6-16, is to discriminate the incoming uplink signal against its carrier. Carrier amplitude detection is also included to generate the enable gate for the control and decode board.

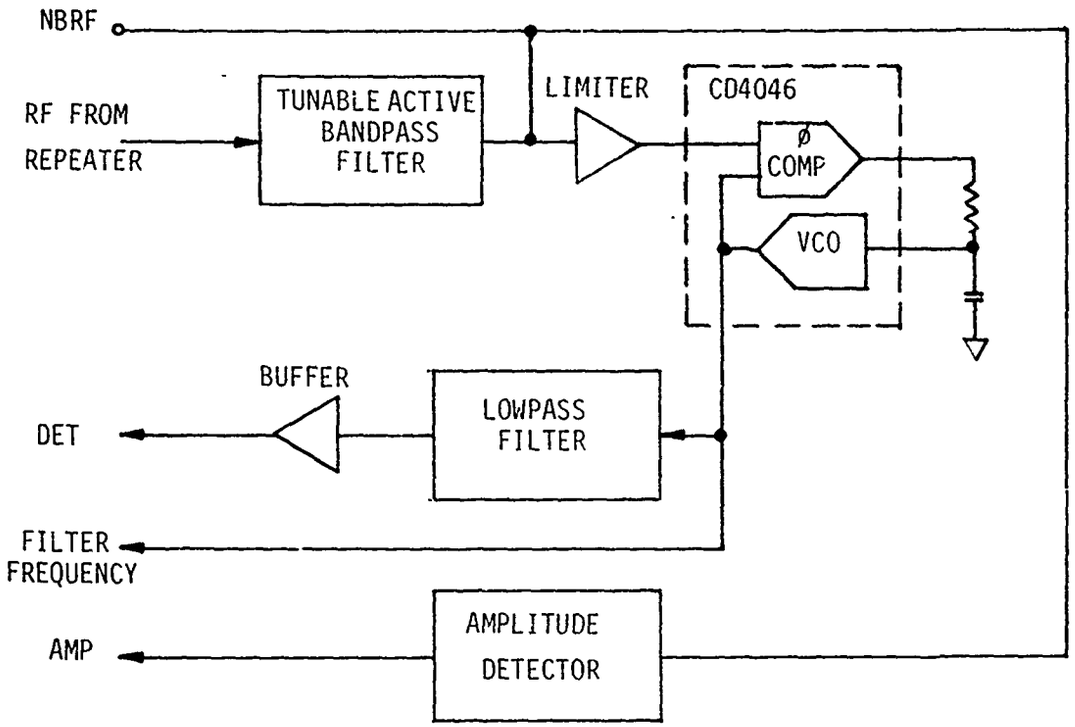


FIGURE 2.6-15
BLOCK DIAGRAM

The tunable input active bandpass filter has two cascaded stages to increase its Q. Flatter frequency response is achieved by degenerative feedback. Matching between the two sections is made by a 1 megohm variable resistor. A front-panel-mounted, two-section potentiometer sets the center frequency of this filter with connections made at Pins 7, 9, and 13. The first stage is implemented with 6D while the second stage is implemented with 4D. Op-amp 2Da provides inverting unity gain for negative feedback to establish the overall filter characteristics. The input filter has an overall gain of two thirds at the center frequency referred to the input at Pin 5. The center frequency of this filter is

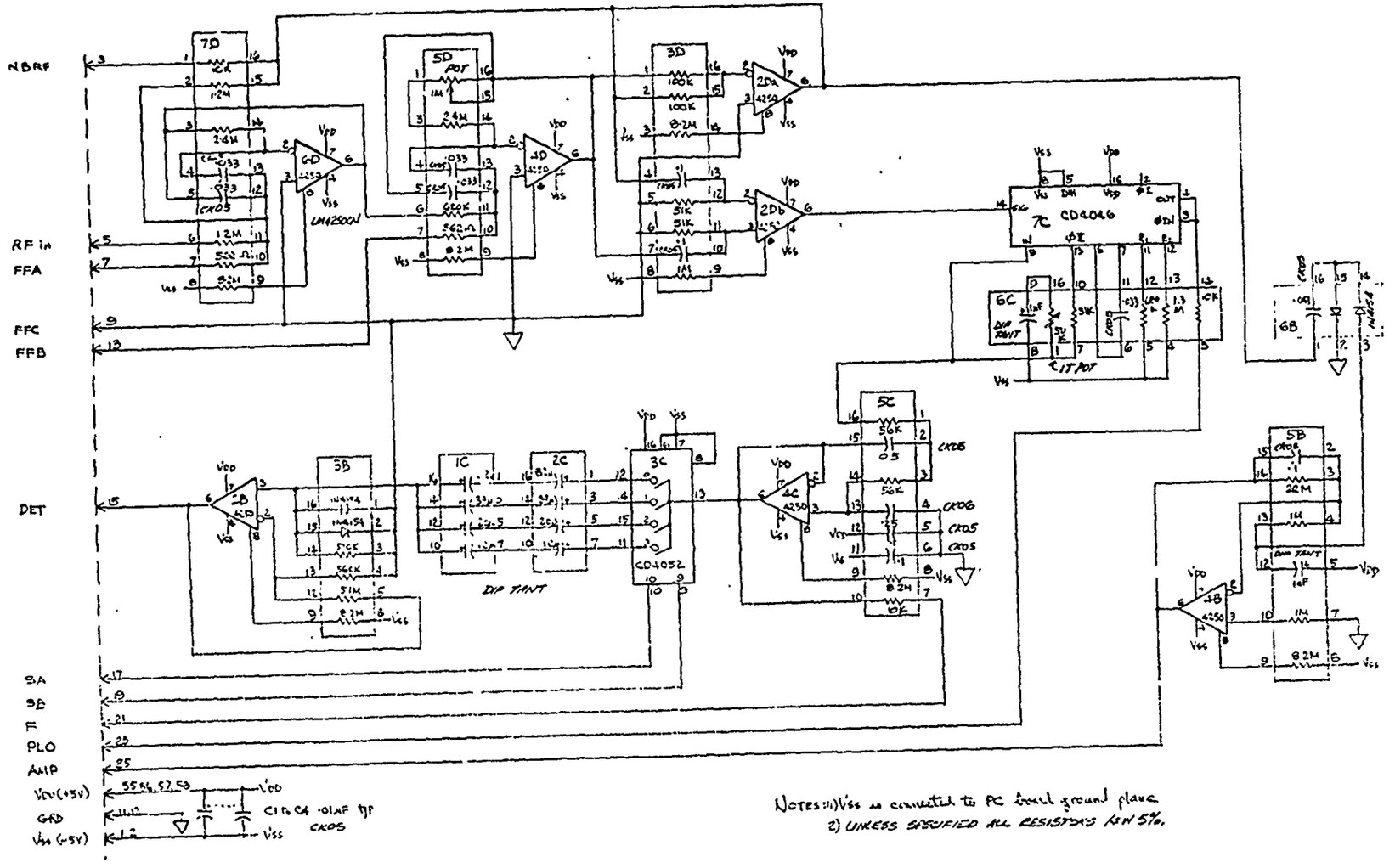


FIGURE 2.6-16

SCHEMATIC, UPLINK DETECTOR, 106068

tunable over the range of 60 Hz to 130 Hz while the bandwidth is fixed at 18 Hz. One of the LM4250 op-amps is used as a limiting amplifier. Differential drive is used to improve the signal-to-noise ratio. The phase lock loop discriminator is an RCA CD4046. It is driven by the limiter directly, and its output feeds an active lowpass filter. The output of the filter is ac coupled to its buffer amplifier. The amplitude detector is implemented with a peak-to-peak rectifier and a gain-of-two amplifier.

2.6.6.4 Timer and Synchronizer Board (105477)

The functions of the timer and synchronizer board are to generate various clock pulses synchronized to the incoming data stream, and to demodulate the incoming data stream. Refer to the block diagram (Figure 2.6-17), timing diagram (Figure 2.6-18), and the schematic (Figure 2.6-19) for the following discussion.

Device 2D and associated components make up the VCO having a nominal frequency of 20480 Hz. The nominal frequency can be adjusted by a front-panel-mounted 10-turn potentiometer. The output of the VCO, C_c, is divided down to C_o by the programmable binary divider formed by devices 2C and 3C.

A 5-position rotary switch mounted on the front panel programs the frequency of C_o which has a nominal value 80 times the incoming data rates. Clock C_o is further divided down by devices 6D and 4D to generate Clock I and Clock Q, square wave signals with I leading Q by 90°. Both of these clocks can be advanced 180° by a phase inverter made up of devices 1C and 3D upon a pushbutton switch command. Clock I triggers the two flip-flops, 5D, which generates clocks CA and CB.

The clocks so derived from the VCO are used to demodulate the incoming signal. The VCO is phase locked to the incoming signal by the loop stress voltage which is a function of the phase relationship between Clock Q and the incoming signal. Half of the bit time of the incoming signal is a "mark"(i.e., a high on the data line); the other half of the bit time is a "space". Data "1" is represented by a "mark" followed by a "space" (1,0). Conversely, data "0" is represented by a "space" followed by a "mark" (0,1). The data line is buffered by an amplifier with complementary outputs made by of 2Aa and 2Ab.

There are three integrations on the timer and synchronizer board. The time constants of these integrators are programmed by the same line that controls the binary divider. The integrator made up of 5Bb and 7Bb, together with the SPDT switch 3B, function as a phase comparator for Clock Q and the data line. When the data line is 90° ahead of Clock Q,

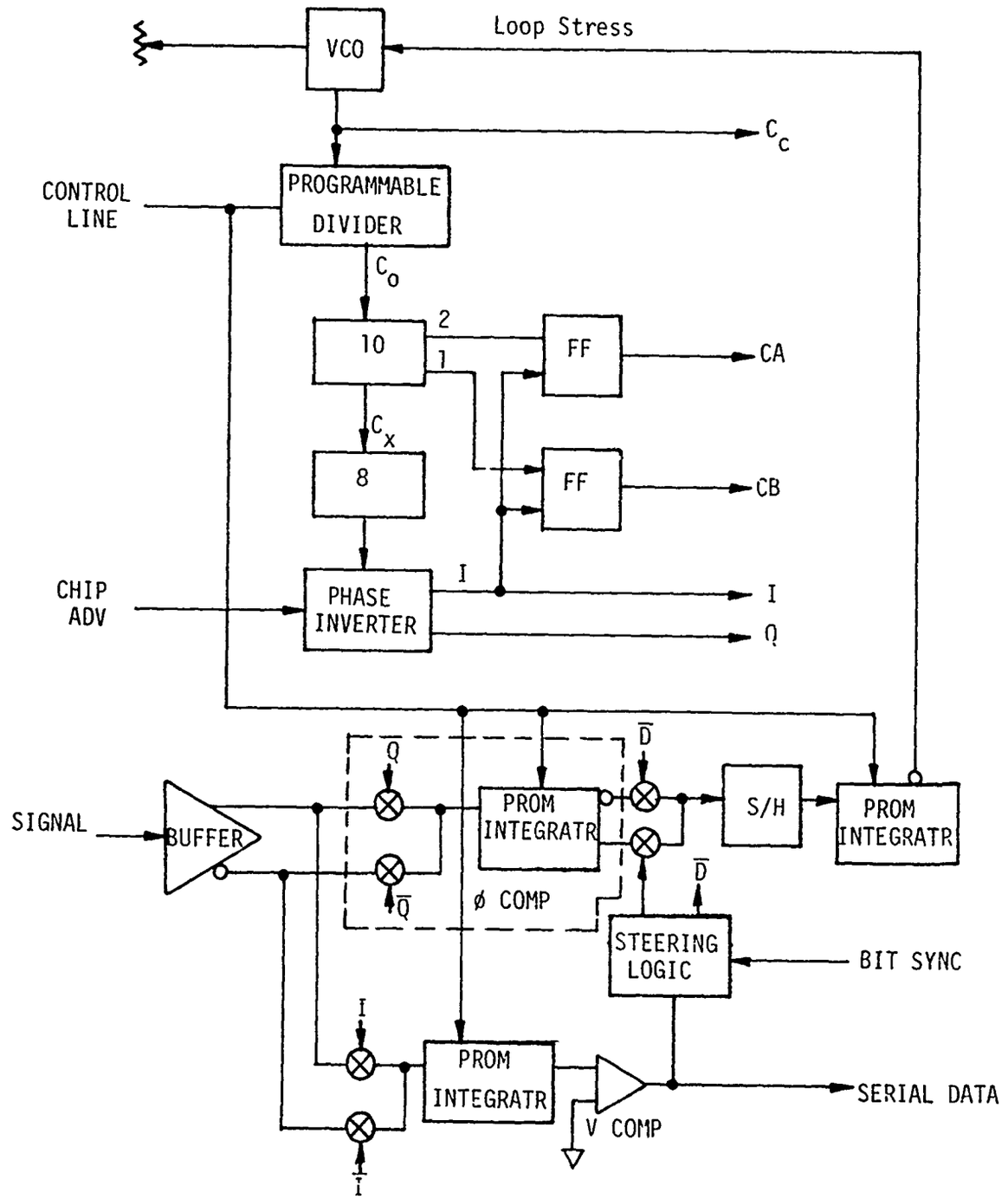


FIGURE 2.6-17
BLOCK DIAGRAM

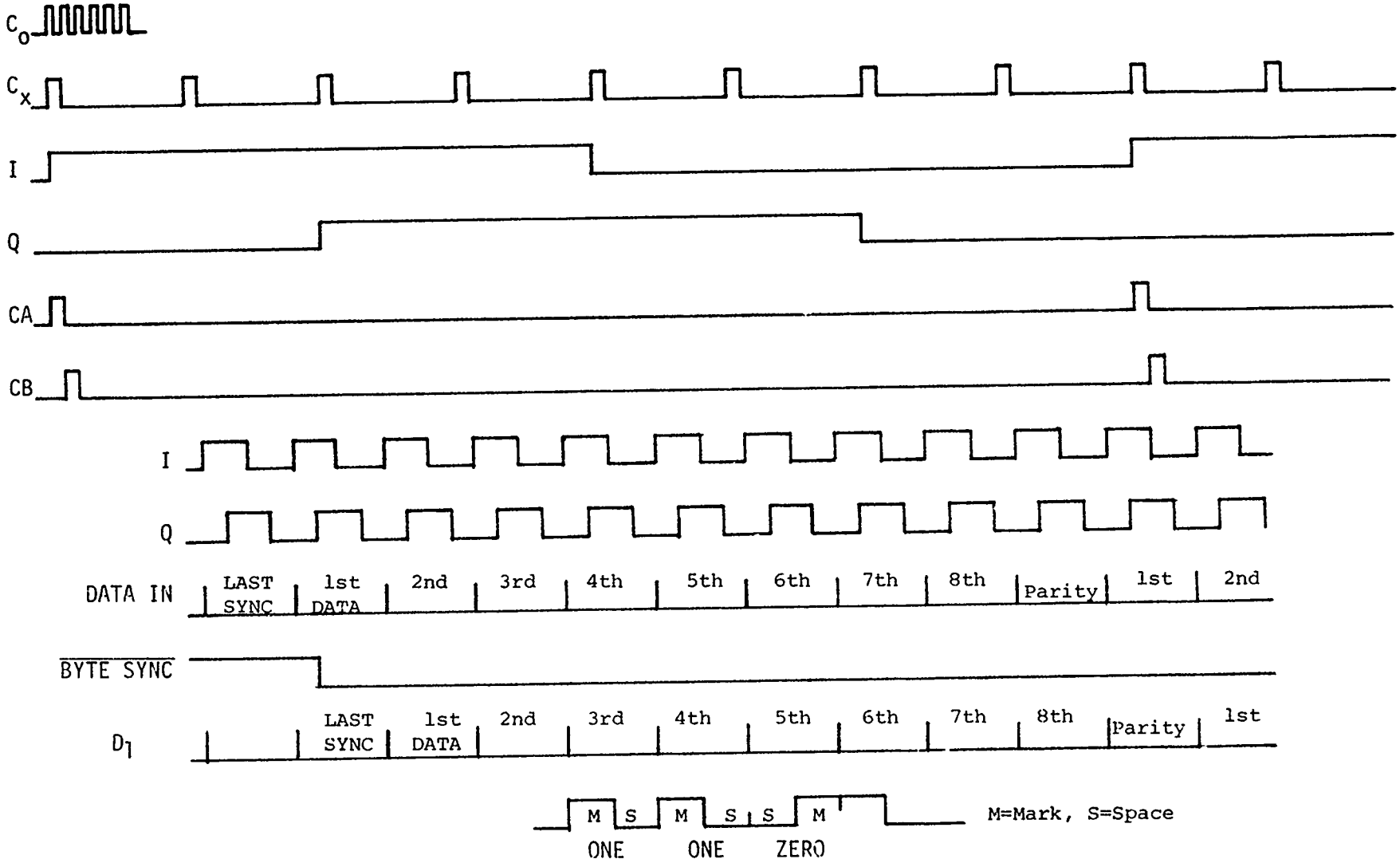
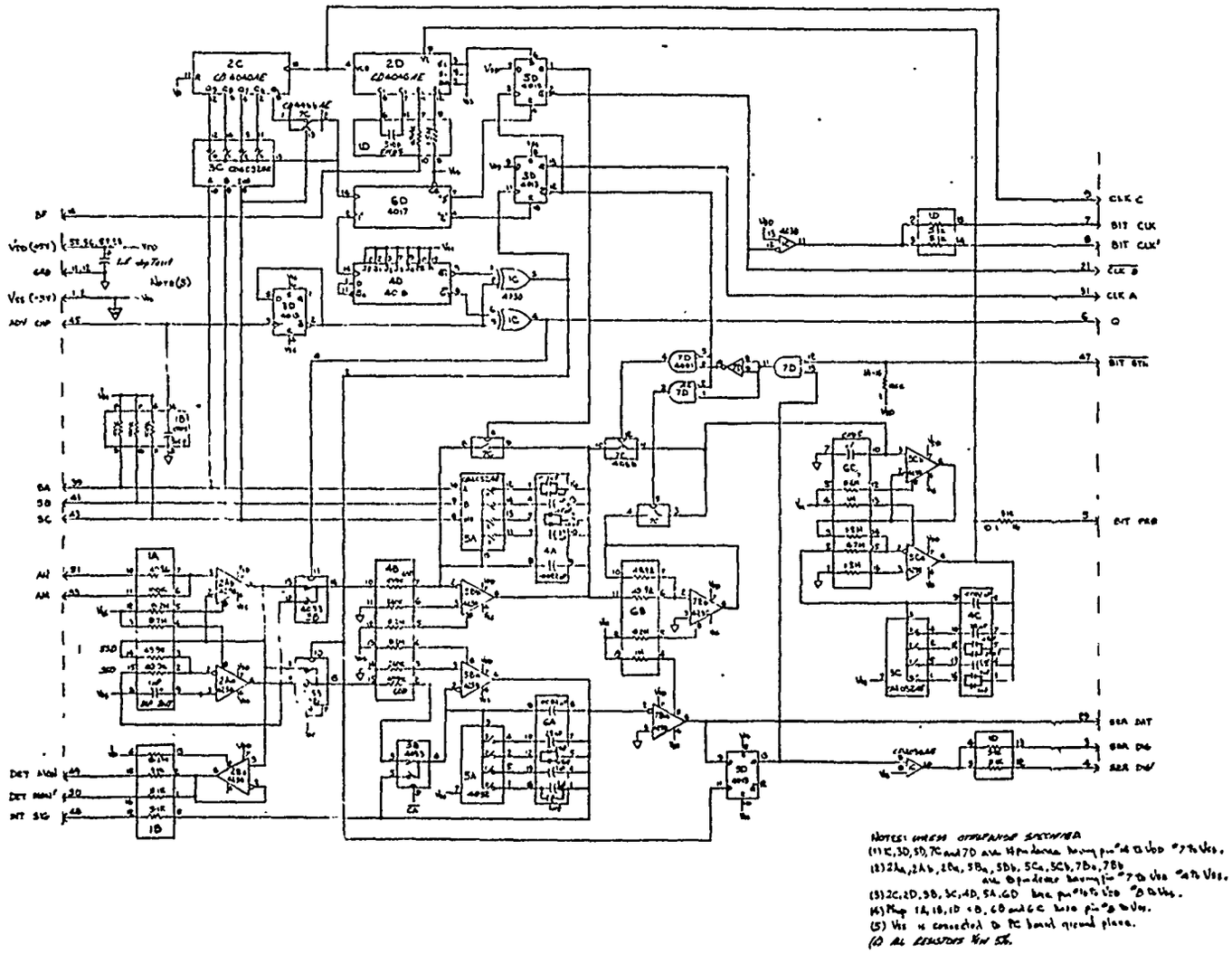


FIGURE 2.6-18

TIMING DIAGRAM



NOTES: UNLESS OTHERWISE SPECIFIED
(1) 1C, 3D, 5D, 7C and 7D are Hamlin hump pin "4 to Vdd "7 to Vss.
(2) 2Aa, 2Ab, 2Ca, 5Ba, 5Db, 5Ca, 5Cb, 7Da, 7Db
all dependent humpline "7 to Vss "14 to Vss.
(3) 2C, 2D, 3B, 3C, 4D, 5A, 6D have pin "14 to Vdd "8 to Vss.
(4) Hump 1A, 1B, 1D + 1B, 6B and 6C into pin "8 to Vss.
(5) Vss is connected to PC board ground plane.
(6) ALL RESISTORS 1/4W 5%.

FIGURE 2.6-19

SCHEMATIC, TIMER AND SYNCHRONIZER, 105477

the output of the phase comparator is zero. When the lead angle is less than 90°, the output is positive if the data is a "1" and negative if the data is a "0". For this reason, the true output is used when the data is a "1", and vice versa when the data is a "0". The steering logic for this function is implemented by devices 7C, 7D, and 3D. Since the first half of the synchronizing preamble is all "1", the steering logic is forced to the true position until BIT SYNC is acquired.

The integrator made up of 5Ca and the sampler made up of 5Cb function as a lowpass amplifier with infinite dc gain to zero in the 90° phase relationship and to provide phase correction from one bit to another bit. The last integrator, 5Ba, and switch, Clock I, together with the voltage comparator, 7Ba, work as the data demodulator. Since both Clock I and the incoming signal lead Clock Q by 90°, Clock I and the incoming data are in phase. Noise rejection and phase margin are optimized by integrating both true and the complement of the incoming data. The uncovered data serve the control and decode board as well as flag the steering logic for the loop stress. A few components are incorporated into this board to provide isolation for the monitor points.

2.6.6.5 Control and Decode Board - 105478

The functions of the control and decode board are to perform serial-to-parallel data conversion, to detect bit and byte synchronization, to perform data parity checks, and various data for the display boards. There are two modes of operation for this board - the normal mode and the force sync mode. Refer to the block diagram of Figure 2.6-20 and the schematic in Figure 2.6-21.

In normal operation, serial data uncovered by the timer and synchronizer board are clocked into a 15-bit shift register (devices 5C and 6C) by clock CA. When seven or all bits of any 8 consecutive bits are "1", voltage comparator A7a will go low; and if Schmitt trigger D2B senses that transmission is on, gate A64 will enable A6 which is the $\overline{\text{BIT SYNC}}$ flip-flop. Byte synchronization is detected in a manner very similar to the acquiring of bit sync with the exception that a series of 15 coded bits is examined. Again, any one of the coded bits could be incorrect; voltage comparator A7B still sees a sync condition, and if bit sync is acquired prior to this condition, gate A3 will enable A5 which is the $\overline{\text{Y SYN}}$ flip-flop. As soon as Y SYN is acquired, the byte counter and the parity checker are enabled to operate.

The byte counter is implemented by 2C and 3C. 3C is normally a decode counter; however, exclusive OR gate 3C generates an extra pulse at the ninth clock, making this counter a divide-by-nine one. In addition, 3C can be made to skip a clock pulse (or bit) by arming Inhibit latch 3B. This latch is self-clearing.

The parity checker is a serial adder, where the result is reset and clocked by the byte clock generated by 3C.

The byte clock, Y CLK, is used by the D/A converter to strobe in the parallel data made available by the serial-to-parallel converter 5C and 6C. Devices 2Da, 4D, 5D and resistor pack 3D. In the same time, the Y CLK also loads the parallel data into the down counter (6D and 7D). The down counter is clocked out by CLK C, which is the output of the VCO located in the timer and synchronizer board.

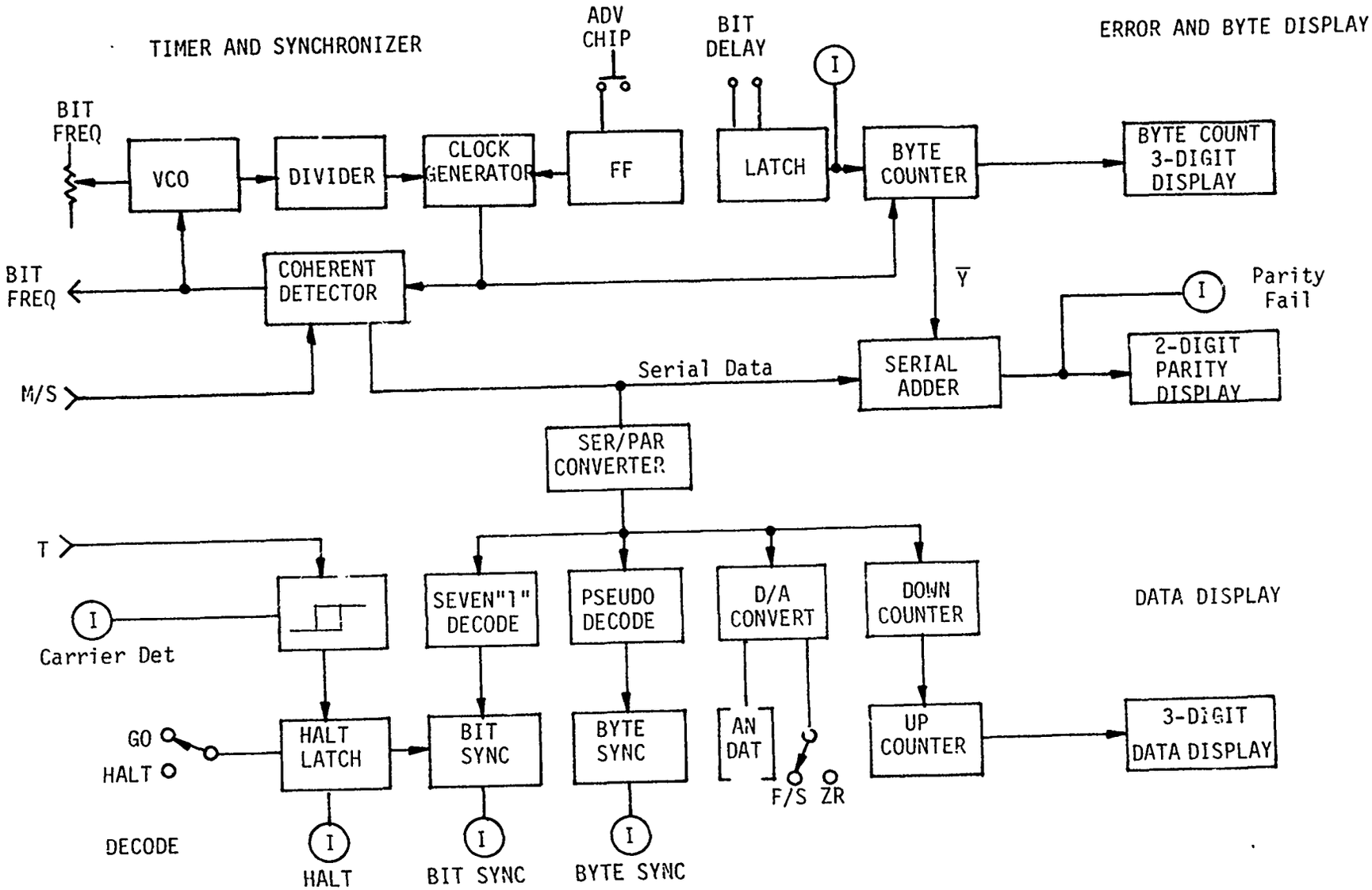


FIGURE 2.6-20

CONTROL AND DECODER BLOCK DIAGRAM

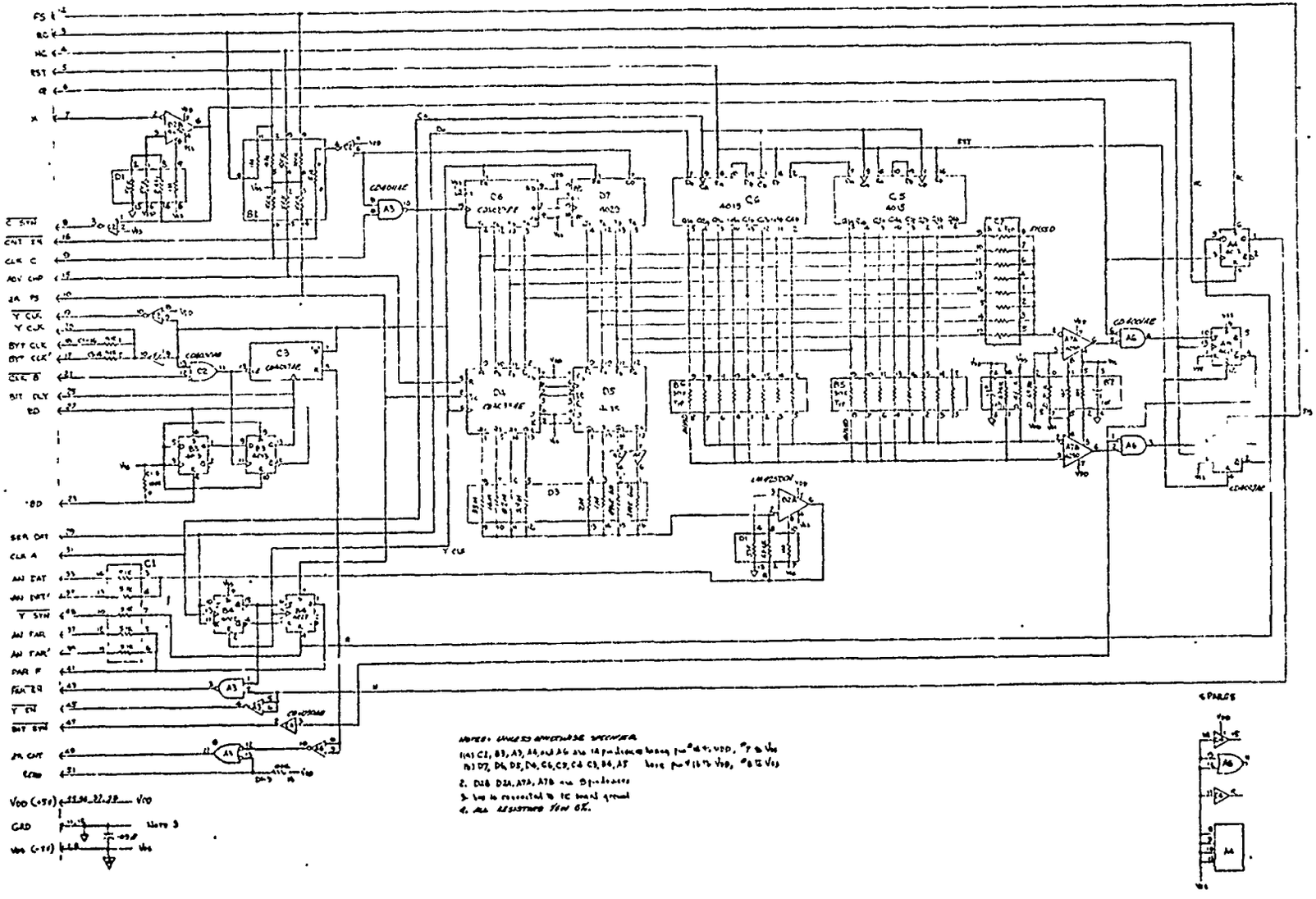


FIGURE 2.6-21

SCHEMATIC, CONTROL AND DECODE, 105478

When the transmission terminates, Schmitt trigger 2Db resets halt flip-flop 4A which in turn stops the parity and byte counter located off board. Halt flip-flop 4A can be set to either resume operation or halt operation through a manual switch.

The other mode of the control and decode board is the force sync mode. The force sync mode is used when the signal-to-noise ratio is so low that a reliable sync acquisition cannot be achieved. In this mode, both the bit sync and the byte sync are bypassed. Byte alignment can be performed by the ADV CHIP and/or the BIT DELAY function.

Various resistors are incorporated in this board for pull-up, pull-down, and isolation purposes.

2.6.6.6 Error and Byte Display - 105475

The error and byte display board, Figure 2.6-22, contains five decidigit displays and three LED indicators. Each digit display is implemented by a decode counter (SN7490), a BCD-to-7-segment decoder and driver (SN7447), a current limiting resistor pack and an LED numeric display. Two of the five numeric displays are used for parity errors, and three of them are designated for the byte counter. Both the parity counter and the byte counter are clocked by the byte clock $\overline{\text{Y CLK}}$; the parity counter is enabled by the $\overline{\text{PAR EN}}$ generated from the parity checker, while the byte counter is enabled by the $\overline{\text{Y EN}}$ which came from the HALT flip-flop.

The three LED indicators used to indicate Parity Fail, Bit Delay, and Halt are driven by a CMOS hex inverter (CD4009). Another CD4009, 3E is used to translate the CMOS logic level (-5 to +5 volts) to TTL compatible logic levels. Note that all the TTL devices are operated off -5 volts.

The display counters are reset by ZR CNT which is the ORed functions of master reset and counter reset.

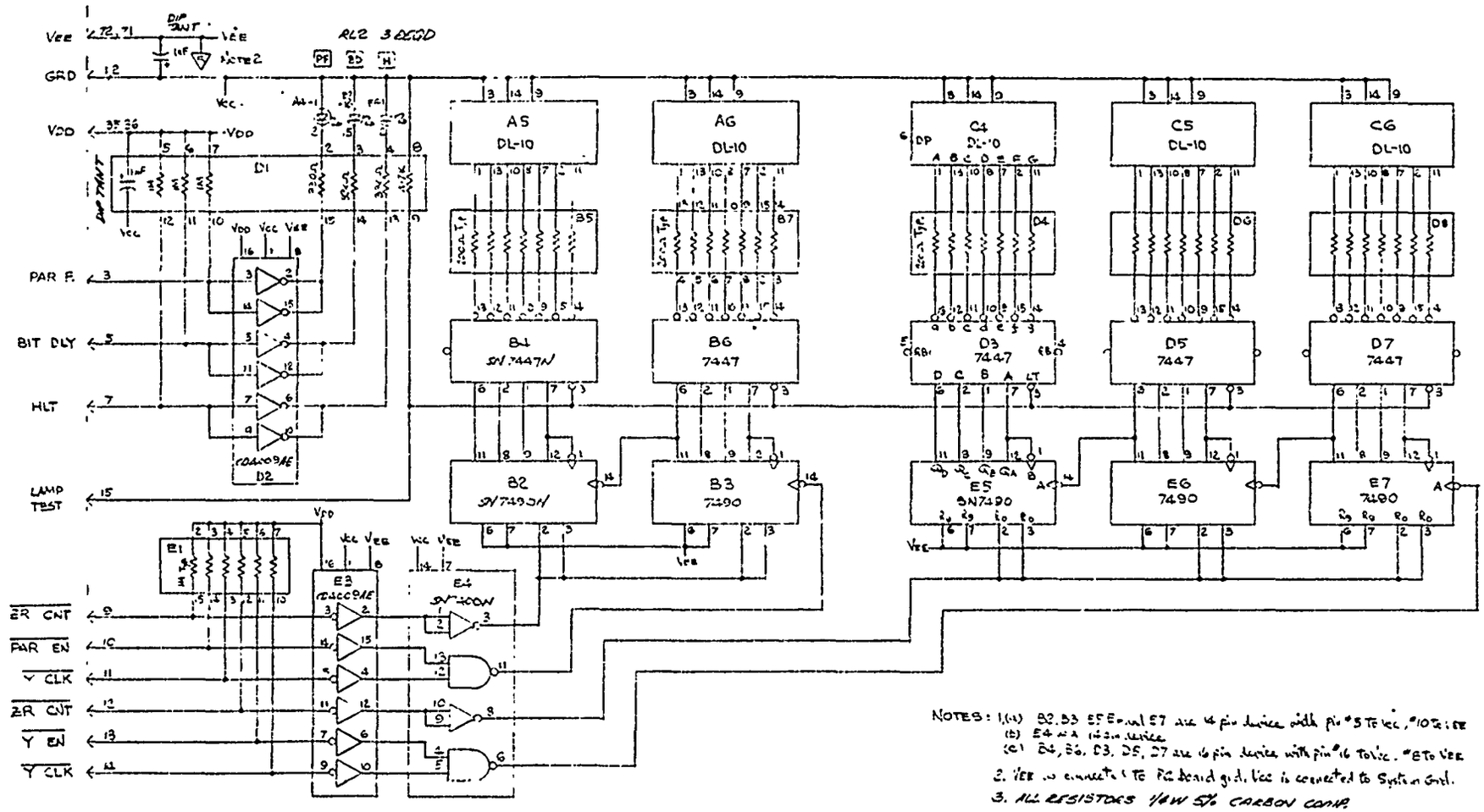


FIGURE 2.6-22

SCHEMATIC, ERROR AND BYTE DISPLAY, 105475

2.6.6.7 Data Display - 105476

The three deci-displays on the data display board, Figure 2.6-23, are similar to those on the error and byte board. This 3-digit display is clocked by CLK C and gated by $\overline{\text{CNT EN}}$ which is generated by the binary down counter in the timer and synchronizer board. Since the display counter is of the decode type, binary-to-BCD conversion is effectively performed for the data. The display counter is reset only by the $\overline{\text{Y CLK}}$.

In addition to the three deci-displays, there are three LED indicators to indicate the acquisition of transmitter carrier, bit and byte synchronization. Similar to the error and byte display board, CMOS hex inverter CD4009 is used to perform logic level translation.

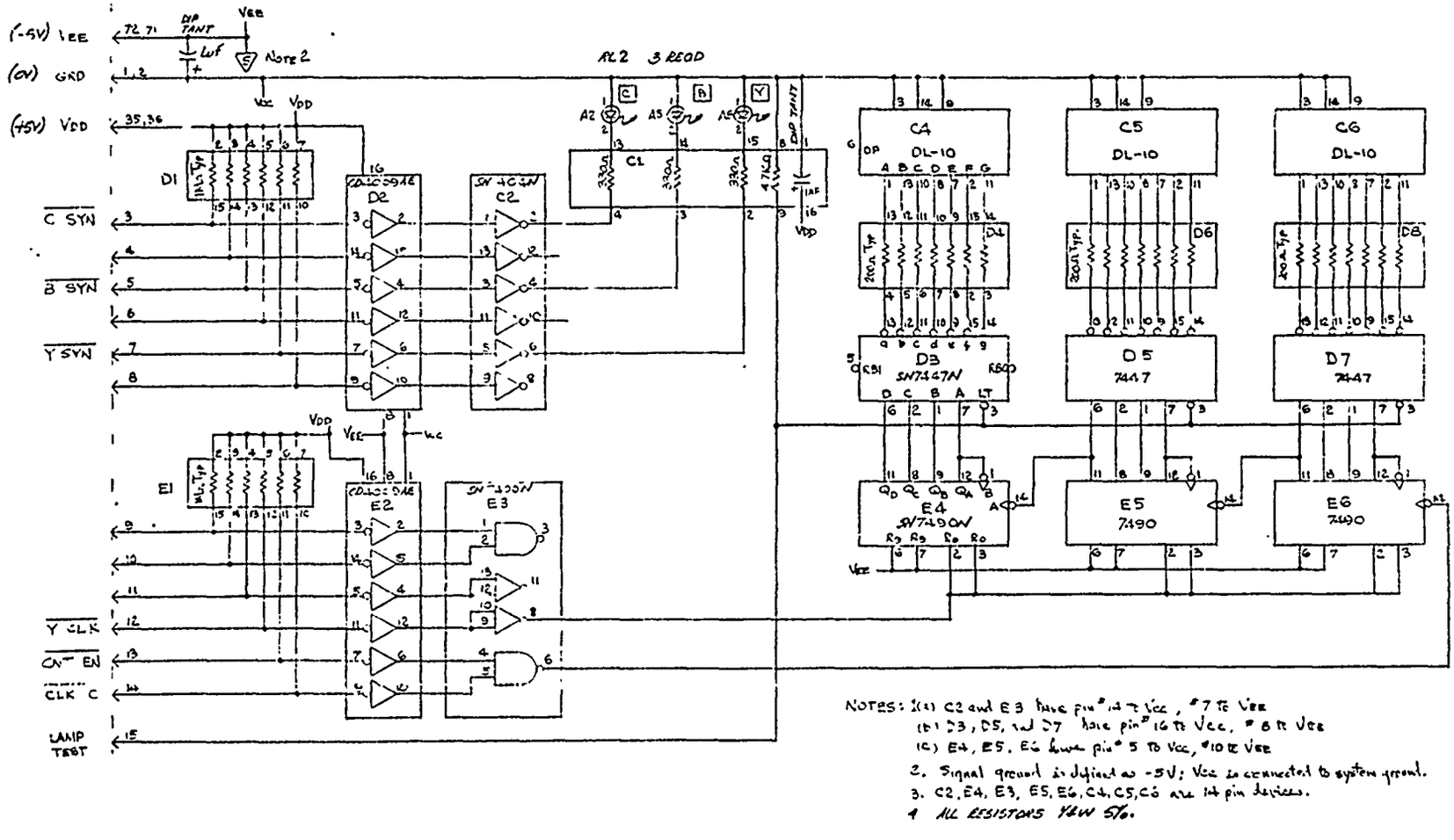


FIGURE 2.6-23

SCHEMATIC, DATA DISPLAY, 105476

3. TRANSMISSION LINK PARAMETERS

Three underground telemetry system downhole canisters were installed as shown in Figure 2.1-2. Transmitting and receiving antennas were deployed on the surface roughly above the downhole units, as shown. A transmitted downlink command from the large surface antenna is used to initiate the uplink data transmission, or dump, which continues at a selectable rate of 0.5, 1, 2 or 4 bits per second until the requested amount of data has been sent. Transmission link design parameters were based on theoretical predictions and were verified by preliminary preshot noise and signal measurements, system checkout during installation and detailed postshot measurements.

The theoretical basis for transmission through the conducting earth medium in this case has been worked out in detail in the Design Definition Report[5] prepared at the beginning of this contract. Since all antennas are basically coaxial, the vertically polarized field at the receiving antennas is given by

$$|H_r| = \frac{m}{4\pi r^3}\,\Gamma_r;$$

$$\Gamma_r = 2\,e^{-r/\delta}\left[1 + 2\frac{r}{\delta} + 2\frac{r^2}{\delta^2}\right]^{\frac{1}{2}}$$

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}$$

where m is the magnetic dipole moment of the transmitting antenna in ampere-turns·meter^2(A·T·m^2), r is the range to the transmitting antennas in meters, δ is the skin depth, and Γ_r is the attenuation constant that is a function of frequency and the earth conductivity σ in siemans(mhos)/meter. A weighted average bulk conductivity of 0.005 S/m to the final installation depths was calculated from resistivity logs for borehole UE12n #9 that is directly over the 210' installation.

3.1 UPLINK PREDICTIONS

The moment of the downhole canister antenna in the transmit mode is approximately 1500 A-T•m^2 (rms) for a power delivered to the antenna terminals of about 14 watts.* Thus, the theoretical uplink signal level, for transmission frequencies around 80 Hz, at the surface for the three cases is

UNIT	r(m)	H_r(μA/m rms)
210'	535	1.6
300'	518	1.7
400'	460	2.7

Uplink reception is limited by ambient power line and atmospheric noise fields since these effects are far greater than preamplifier noise. The worst-case model for the horizontal field of atmospheric noise is

$$H_{nA} = \sqrt{10^{-11}/f} \quad A/m$$

and the vertical component, which is the one of interest for the receiving loops in this case, is typically 10 to 20 dB less depending upon conditions. Since the post-detection receiver bandwidth is 2 Hz (1/2 the baud rate of 4 bits per second typically used), the effective vertical noise field at 80 Hz is less than 0.16 μA/m. Thus, the theoretical SNR for the atmospheric noise limited case will be better than 19 dB, which is adequate for code reception. Consideration of the uplink receiver bandwidths and notch filter attenuations results in estimates of power line interference tolerances for greater than 20 dB SNR as follows:

60 Hz	< 64 μA/m rms
120 Hz	< 20 μA/m
180 Hz	<640 μA/m

Detailed measurements of the uplink noise conditions and signal parameters were made after the post-shot operations as described in the next section.

*Reference Page 2-130.

3.2 UPLINK TRANSMISSION MEASUREMENTS

Follow-up field operations were conducted on 10 and 11 June 1976, approximately one month after the event and post-shot data dump operations to measure the uplink transmission parameters and verify performance predictions.

Power conditions were opposite to what they had been post shot. The large diesel generator in the power van was not working and commerical power was on and driving the motor generator sets. This was thought to be a worse condition, but the differences are probably not too significant based on the low uplink transmission parity error rates observed.

Downlink command conditions were also nearly identical to those post shot. The weather was cumulus clouds and light showers, but no apparent lightning, so atmospheric noise conditions were probably average.

3.2.1 Received Signal Measurements

The uplink antenna and receiving system, Figure 3.2-1, was calibrated by installing a single-turn source field coil, coaxial and coplanar with the receiving antenna, and driving it with a known current. The calibrate current, I_c, produces a receiving antenna output voltage, V_c, of

$$V_c = j\omega M I_c$$

where $\omega/2\pi$ is the operating frequency and M is the mutual inductance of the two loops.[7] This can be related to the output produced by a equivalent uniform magnetic field, H_c, by

$$V_c = j\omega N A_e \mu_0 H_c$$

where N=2 is the number of turns in the antenna coil, A_e is the area of the antenna loop or $\frac{\sqrt{3}}{4} a^2 = 9.04\ m^2$, and $\mu_0 = 4\pi \times 10^{-7}$ H/m.[9]

The field strength of the signal, H_s, can then be calculated from the receiver output V_s by

$$H_s = \frac{H_c}{V_c} V_s = \frac{M I_c}{N A_e \mu_0 V_c} V_s \quad (A/m)$$

The calibrating current is essentially the short output current of the 600 ohm attenuator which is

$$I_c = (\frac{V_{in}}{31.6})(\frac{2}{600}) = 1.05 \times 10^{-4} V_{in} \quad \text{(amperes)}$$

for a 30 dB attenuator setting.

For coaxial triangles very close together, the mutual inductance can be calculated from the following approximate series formula:[10]

$$M = 0.006\ S[\ell og_e \frac{S}{d} - 1.4055 + 2.209 \frac{d}{S} - \frac{11}{12} \frac{d^2}{S^2} + \frac{203}{864} \frac{d^4}{S^4} - \ldots]$$

where S is the triangle side length in centimeters, d is the distance between their planes in centimeters and M is in microhenries. The mutual in-

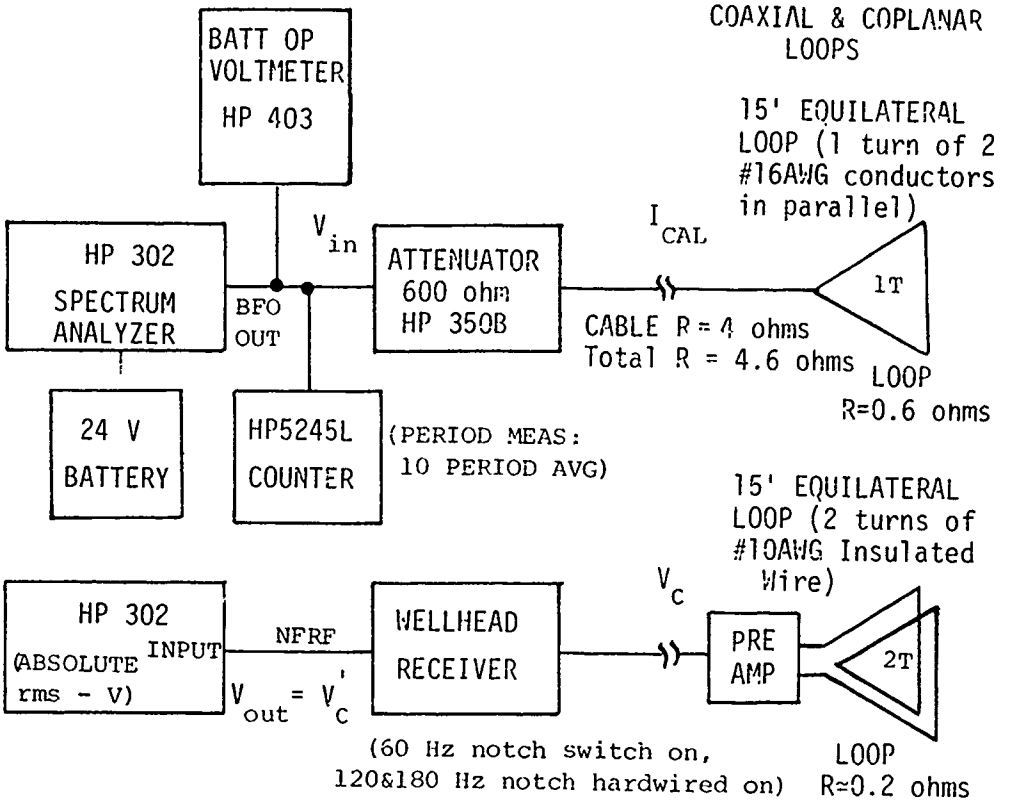


FIGURE 3.2-1

UPLINK RECEIVER - PREAMP / ANTENNA FIELD CALIBRATION

ductance rapidly increases as the distance between the loops is decreased and ultimately approaches a limiting value of $M_0 = \sqrt{L_1 L_2}$ where L_1 and L_2 are the inductances of the two coils, or about 38 microhenries in this case.[11]

It was not possible to achieve a uniform, precise and measurable arrangement of the two loops under the field conditions, so it is only possible to calculate an approximate value of M. Since it is estimated that the two loops were within about 1 inch (2.54 cm) of each other on the average, the actual mutual inductance is on the order of 20 microhenries.

The field calibration results are given in Table 3.2-1 for frequencies near those of the uplink transmissions. Note that the receiver output voltages were measured at a point after the power line notch filters, i.e., NFRF,

but before clipping, and the levels are below saturation. The overall frequency response of the wellhead receiver, preamplifier and antenna system were quickly checked at the same time, and the results are shown in Figure 3.2-2. The measurements at the notch frequencies are approximate only since there was difficulty in determining the notch minimums even though the calibration output voltage appears to be higher than the background noise. Both the laboratory measurements and the later measurements of received noise suggest the effective notch attenuation is greater than indicated.

TABLE 3.2-1

UPLINK RECEIVER - PREAMP/ANTENNA FIELD CALIBRATION RESULTS

FREQUENCY Hz	V_{in} Vrms	ATTENUATOR SETTING dB	I_c μA	V_c' * Vrms	H_s/V_s' A/m/Vrms
71.4	1.33	30	140	1.03	1.20×10^{-4}
76.3	1.32	30	139	1.15	1.07×10^{-4}
80.0	1.32	30	139	1.20	1.03×10^{-4}
85.5	1.32	30	139	1.23	1.00×10^{-4}
90.9	1.32	30	139	1.25	0.99×10^{-4}

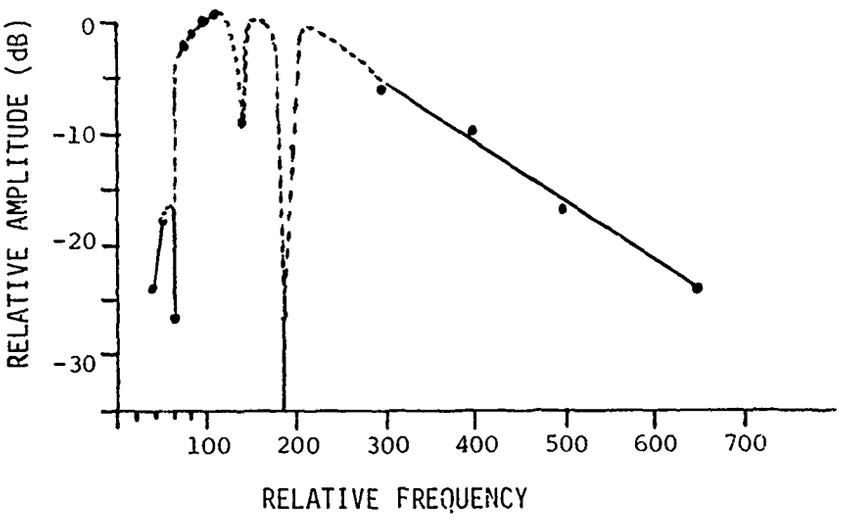


FIGURE 3.2-2

FIELD MEASUREMENTS OF RELATIVE FREQUENCY RESPONSE OF UPLINK RECEIVER-PREAMP/ANTENNA SYSTEM

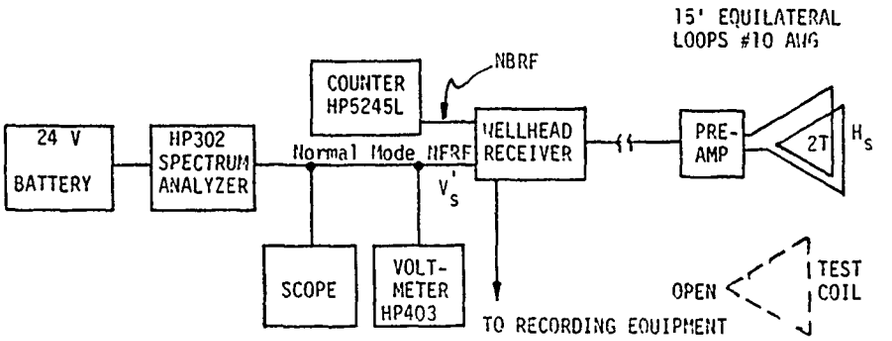


FIGURE 3.2-3
UPLINK TRANSMISSION MEASUREMENTS

The measurement of the uplink signal amplitude and frequency was done as shown in Figure 3.2-3. Each system was commanded to transmit the preamble and three bytes of housekeeping data at 0.5 bit per second to allow time to make the measurements. The tape recorder was turned off to eliminate its high frequency components from the broadband monitors (scope, voltmeter). Even so, the background noise was too high for the broadband data to be of value although the signal could be observed.

The transmitted frequency was measured by connecting a counter to the NBRF output (post clipping and narrowband filtering), which provides a 1.5 to 2 volt p-p sine wave, and taking the average of 10 periods (approximately 0.125 s) per sample. Since the mark or space frequency of the PCM signal lasts for 1 or 2 seconds (depending on the bit sequence) at 0.5 bps, this gives about 8 or 16 samples at each frequency. The measured values, Table 3.2-2, were reproducible and consistent. Although the frequency values are slightly higher than those measured in the lab, they are believed to be essentially the same as the installed preshot values since it was not necessary to make any changes in the receiver frequency settings. (The differences are believed to be due to detuning caused by proximity to steel in the laboratory.)

TABLE 3.2-2

UPLINK TRANSMISSION FREQUENCIES

		210'		300'		400'	
	NOMINAL	LAB	FIELD	LAB	FIELD	LAB	FIELD
SPACE	80 Hz	78.7	81.3	79.4	82	78.7	80
MARK	84 Hz	82.6	85.5	84.8	86	83.3	84

The signal (plus noise) levels shown in Table 3.2-3 were measured at the NFRF output (post notch filter, preclipping) using the HP302 Spectrum Analyzer. Since the spectrum analyzer has a 7-Hz bandwidth, it was relatively easy to track the 4-Hz changes, which occurred every 1 or 2 seconds, of the PCM signal. The signal levels were consistent at each frequency and the broadband measurements (scope) are roughly consistent with those monitored in the post-shot operations. Although noise fluctuations introduced a several millivolt uncertainty, the measured signal is reasonably accurate for comparison purposes. The equivalent field strength is calculated using the calibration data above and is in reasonable agreement with predicted values in Section 3.1.

TABLE 3.2-3

UPLINK SIGNAL LEVELS

TELEMETRY CANISTER	SIGNAL + NOISE NFRF RCVR OUT (mV rms; 7 Hz BW)	SIGNAL + NOISE FIELD STRENGTH (μA/m rms; 7 Hz)
210'	20	2.04
300'	20	2.04
400'	30	3.06

The noise at the NFRF receiver output was roughly measured before and after each transmission and typical values, measured with the HP302 Spectrum Analyzer, are given in Table 3.2-4. Narrowband otuput noise at the signal frequencies is consistent with the atmospheric noise measurements (see Table 3.2-7). There did not appear to be any significant noise components at 60, 120 and 180 Hz, the levels being only slightly higher than

the background noise at surrounding frequencies if at all, based on a rough check with the tape recorder off (no narrowband measurements were made with the recorder on). Note that the levels of power line noise measured at the antenna should be observable, at least at 60 and 120 Hz, if the notch filter calibration in Figure 3.2-2 was correct, suggesting the actual notch attenuation is higher.

TABLE 3.2-4

NOISE LEVELS AT WELLHEAD RECEIVER

FREQUENCY Hz	NFRF RECEIVER OUTPUT mV rms; 7 Hz BW (HP302)
60	≈1 mV avg to 2 or 3 mV (about the same as the background)
80-85	≈3 mV avg (some peaks to 5 mV & occasional sharp peaks to 10 mV) or ≈0.3 μA/m equivalent field strength
120-180	≈3 mV avg to 5 mV (no significant change in amplitude of background noise)

Although it was not possible to obtain satisfactory noise measurements at the receiver, for all frequencies and conditions of interest, the summary of broadband levels recorded from the oscilloscope in Table 3.2-5 show the differences were not too significant. For example, it did not seem to make any difference whether the tape recorder was on or off (coax cables were always connected to the receiver for recording various functions) unless the NFRF output was connected to the recorder and this is thought to be due to feedthrough of the higher frequency recorder carrier on the signal line. However, they are eliminated in the narrowband filtering as observed at the NBRF output. The sferics were infrequent and on the order of 6 to 10 dB higher than the general background noise so were not a factor. Turning the 60-Hz notch filter off gave an increase in noise level that is consistent with the 60-Hz level measured at the antenna/preamplifier. Based on these observations, the noise at the receiver appears to be due only to the noise fields at the antenna and the system is in fact atmospheric noise limited.

TABLE 3.2-5

SUMMARY OF BROADBAND MEASUREMENTS AT RECEIVER NFRF OUTPUT

(with 60-Hz notch filter on except as noted)

TIME	LEVEL AT NFRF OUTPUT	CONDITION
6/10 pm	≈100 mV p-p typical >300 mV p-p bursts (sferics)	NOISE. Recorder on and not connected to NFRF.
	≈200 mV p-p typical	SIGNAL + NOISE Canister #4, recorder on and not connected to NFRF.
	≈100 mV p-p typical >300 mV p-p bursts	NOISE. Recorder on and not connected to NFRF.
	≈200 mV p-p typical	NOISE. Recorder on and connected to NFRF (re feedthrough or recorder carrier).
	≈300 mV p-p typical	SIGNAL + NOISE. Canister #2, recorder on and connected to NFRF.
6/11 am	All of the following measurements made with tape recorder off.	
	≈100 mV p-p typical	NOISE
	≈150 mV p-p typical	SIGNAL + NOISE Canister #4
	≈75 mV p-p typical	NOISE
	≈125 mV p-p typical	SIGNAL + NOISE Canister #2
	≈75 mV p-p typical	NOISE
	≈125 mV p-p typical	SIGNAL + NOISE Canister #1
	≈75 mV p-p typical	NOISE
	≈125 to 150 mV p-p typ	SIGNAL + NOISE Canister #4 (repeat)
	≈75 to 100 mV p-p ≈200 mV bursts	NOISE (Slow sweep)
	≈500 mV p-p	NOISE with 60-Hz notch filter off (120 & 180 Hz Notches are always on.)

3.2.2 External Noise Environment Measurements

Measurements of power line and atmospheric noise fields were made right at the antenna and preamplifier, using a battery operated HP302 Spectrum Analyzer, in order to evaluate overall system performance. The field response of the antenna/preamplifier was calibrated using the same general setup and theory as described above for the signal measurements, except the measurements were made at the preamplifier as shown in Figure 3.2-4. The field calibration data is given in Table 3.2-6 and plotted in Figure 3.2-5 for interpolation.

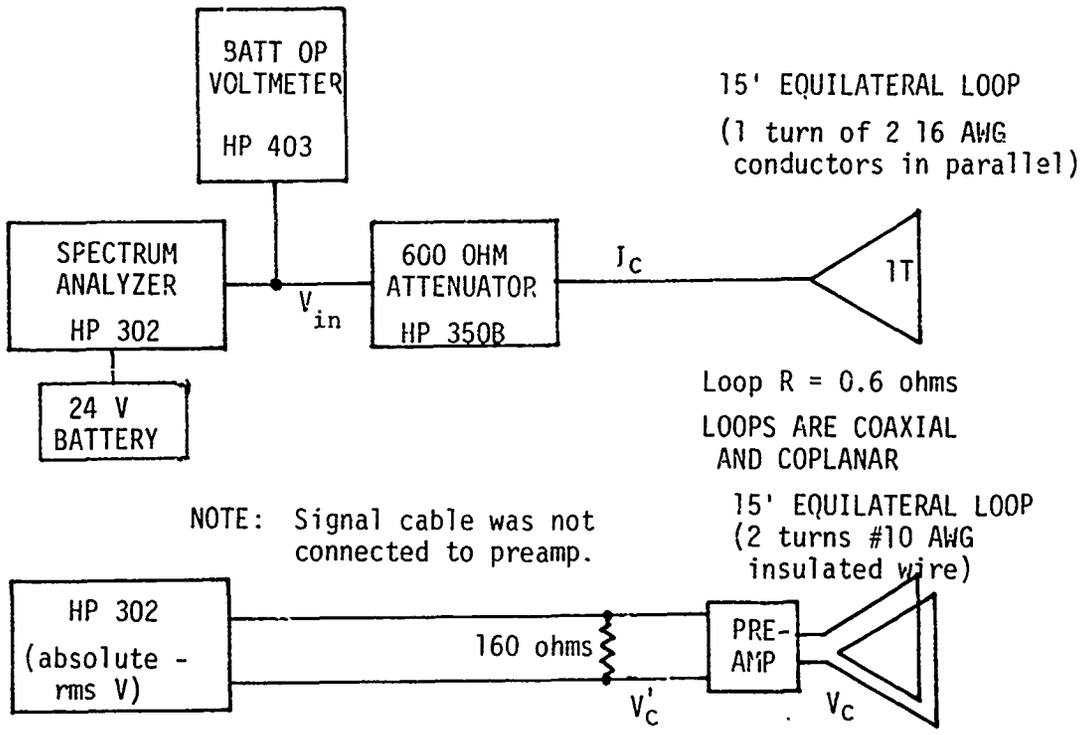


FIGURE 3.2-4
PREAMP/ANTENNA FIELD CALIBRATION

The frequencies are approximate since the spectrum analyzer drifted considerably and adjustments were made from drift estimates based on dial readings during the power spectrum measurement and a post-test frequency

TABLE 3.2-6

ANTENNA/PREAMPLIFIER (ONLY) FIELD CALIBRATION

APPROXIMATE FREQUENCY (Hz)	INPUT VOLTAGE V rms	ATTENUATOR SETTING (dB)	CAL CURRENT (μA)	OUTPUT* VOLTAGE V rms	FIELD CALIBRATION A/m/V
25	1.35	30	142	0.003	4.17×10^{-2}
57	1.38	30	145	0.015	0.85×10^{-2}
80	1.38	30	145	0.028	4.57×10^{-3}
128	1.38	30	145	0.060	2.13×10^{-3}
177	1.38	30	145	0.100	1.28×10^{-3}
230	1.38	30	145	0.130	0.98×10^{-3}
280	1.38	30	145	0.150	0.85×10^{-3}
380	1.38	30	145	0.168	0.76×10^{-3}
485	1.38	30	145	0.150	0.85×10^{-3}
585	1.38	30	145	0.120	1.07×10^{-3}
1250	1.38	30	145	0.015	0.85×10^{-2}

*All levels are below preamplifier saturation

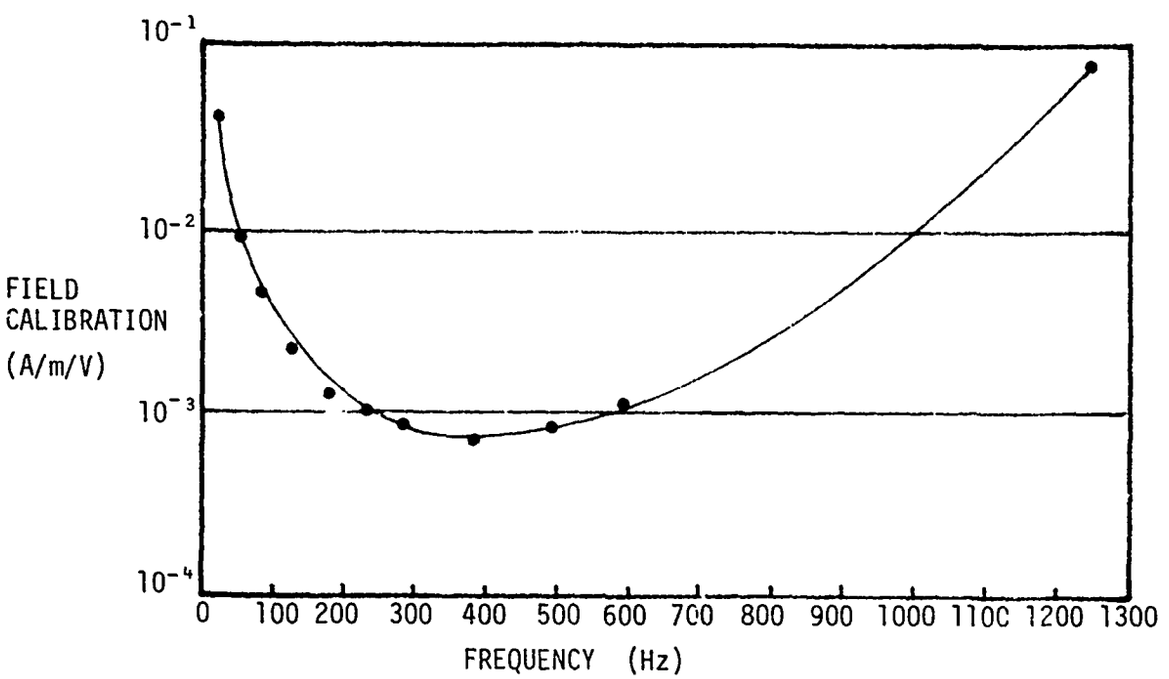


FIGURE 3.2-5

ANTENNA/PREAMPLIFIER FIELD CALIBRATION vs. FREQUENCY

check in the recording van. However, the frequencies are believed to be nearly correct since the two methods of checking drift were consistent. Also, the wellhead receiver gain calculated from the receiver and preamplifier calibration data at 100 Hz agrees with the previous measurements and is a good check because of the sharp preamplifier (only) response at these frequencies.

The noise output of the antenna/preamplifier was measured as shown in Figure 3.2-6, and the results are given in Table 3.2-7. All readings were made with the receiving antenna in its normal position and no attempt was made to find the direction of maximum noise. The measurements were first made with the signal cable connected to the preamplifier and its shield connected to the wellhead receiver ground (but no connection of the signal lines to the receiver) and then with the signal cable disconnected from the preamplifier to determine if there was any noise pickup in the cable shield. The results were essentially the same for either condition with only slight differences that were within the normal fluctuations. The tabulated values of field strength are averages of the typical levels and do not include the peaks due to sferics, etc. All readings were reproducible and those at 60 Hz and the signal frequencies are consistent with the levels measured at the wellhead receiver.

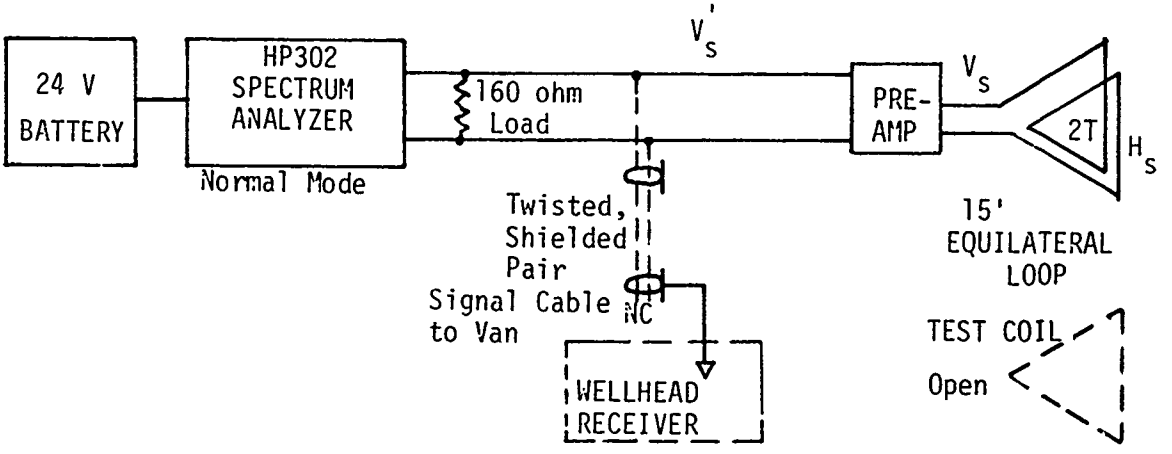


FIGURE 3.2-6

EXTERNAL NOISE ENVIRONMENT MEASUREMENTS

TABLE 3.2-7

NOISE LEVELS AT ANTENNA/PREAMP

(with cable disconnected)

FREQUENCY (Hz)	PREAMP OUTPUT mV rms; 7-Hz BW	AVERAGE NOISE FIELD AMPLITUDE (μA/m rms; 7 Hz BW)
60	3 to 5	≈24
60 to 120	<0.1	<0.37 at 90 *
120	1 to 1.5	≈3.1
120 to 180	<0.2	<0.32 at 150
180	15	≈19
180 to 240	<0.2	<0.21 at 210
240	0.5 to 0.6	≈0.52
240 to 300	<0.2	<0.17 at 270
300	4 to 5	≈3.69
300 to 360	0.1 to 0.2	<0.12 at 330
360	0.4 to 0.6	≈0.38
360 to 420	0.1 to 0.2	<0.12 at 390
420	2 to 2.5	≈1.76
420 to 480	0.1 to 0.2	<0.12 at 450
480	0.2 to 0.4	≈0.25
480 to 540	0.1 to 0.2	<0.13 at 510
540	2 to 2.5	≈2.12

*Observed occasional sharp increases of noise (sferics) at most intermediate frequencies, but no data on amplitude.

3.2.3 Comparison with Theoretical Predictions

Measured signal strengths were all slightly above, but within 3.5 dB of, the predicted values as shown in Figure 3.2-7. At the same time, the natural noise level was slightly higher than predicted. Both effects could be the result of a calibration error. It seems quite likely, however, that the noise level was high because of the placement of the receiving antenna on a hillside, which diverted its axis from vertical, resulting in less polarization gain than the expected 10 to 20 dB. Also, the signal discrepancy could be the result of the gradient in conductivity, which tended to increase with depth. This tapered wave impedance could result in a lower loss than the constant impedance model used.

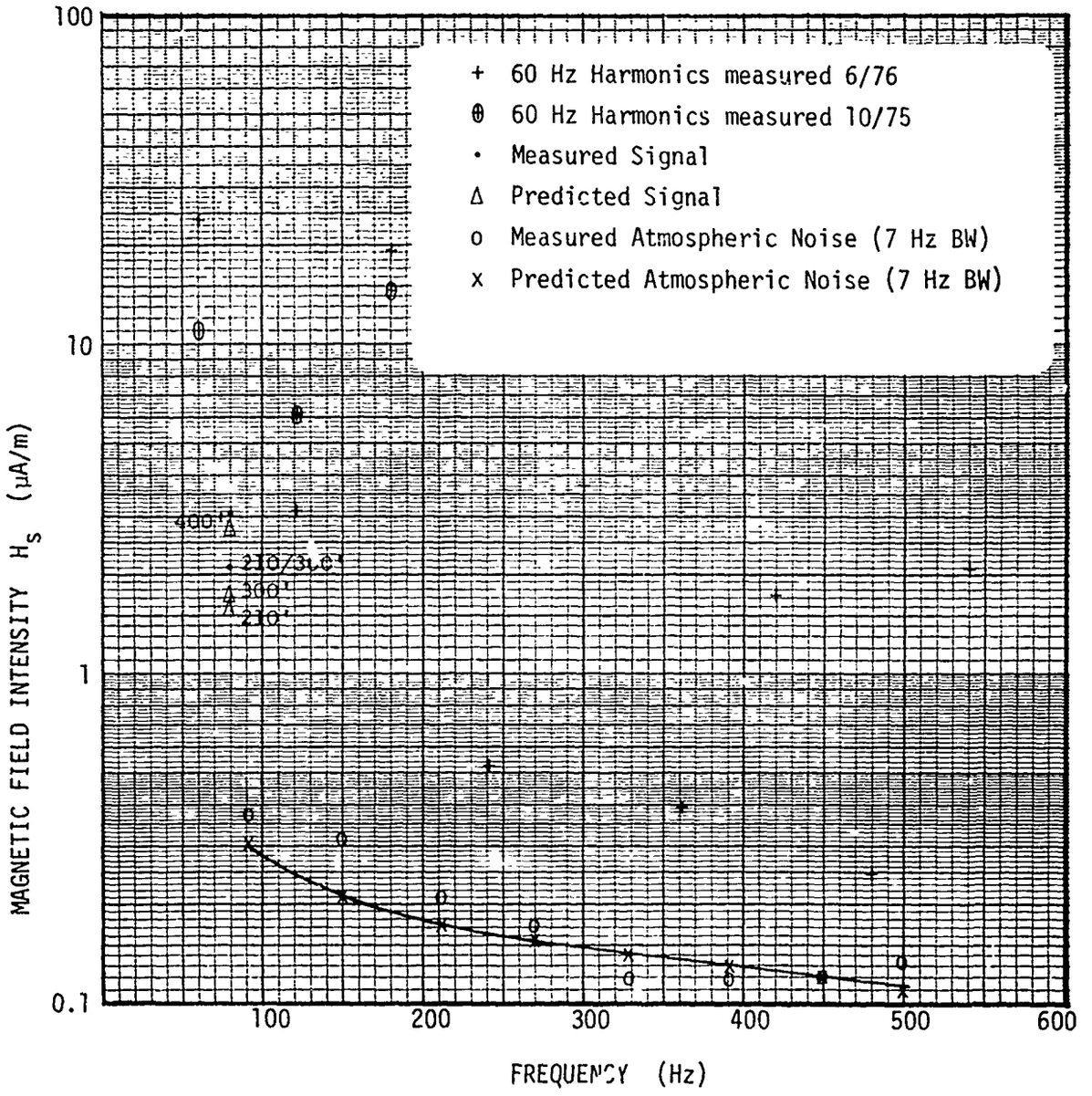


FIGURE 3.2-7

MEASURED AND PREDICTED FIELD STRENGTH

3.3 DOWNLINK PREDICTIONS AND PERFORMANCE

Consideration of downlink performance is somewhat different since power line and atmospheric noise is normally attenuated somewhat so that reception could be limited by the downhole canister receiver front end noise. This system was designed for operation to depths of 2500 feet (763 m) with 0.05 S/m conductivity. Under these conditions, the atmospheric noise would have been about 4×10^{-9} A/m$\sqrt{\text{Hz}}$, still about 16 dB above the set noise level of about 6×10^{-10} A/m$\sqrt{\text{Hz}}$. In addition, early measurements indicated that very high levels of power line noise could be expected due to tunnel construction activities that would interfere with preshot checkout, but would not exist under post-shot conditions. Also, transients were found to couple into the front end when the MPU turned on, creating an effective noise level 30 to 40 dB above set noise although the net effect was significantly reduced by receiver blanking during this brief time. Thus, a very large surface transmitting antenna was chosen to insure sufficient signal strength at the downhole receiver under all conditions. A secondary reason for the choice of a large antenna was the possibility of post-shot receiver degradation due to shock. It turned out the transmitter size was excessive on both counts.

The surface transmitting antenna, made from 4-conductor #8 AWG power cable, was laid out on the rough, but relatively flat (±70 feet or 21 meters), terrain in the form of a multisided polygon roughly approaching a circle. The total circumference is close to 3200 feet (976 meters) although the effective radius for area calculations is probably in the range of 400 to 510 feet (120 to 153 meters). The inductance of the 4-turn loop thus formed calculates to be about 36 mH so the reactive impedance around 90 Hz is larger than the total resistance of 8 ohms and must be considered in power calculations based on voltage measurements. Thus, the magnetic dipole moment for various drive voltages used in test and actual operations falls somewhere in the range of values indicated in Table 3.3-1, depending on the exact antenna area which is not precisely known.

At the time of the installation of the first system (the 400' unit), tests were conducted to determine the required level for downlink transmitter operation and make simultaneous measurements of signal and noise in the

TABLE 3.3-1

DOWNLINK TRANSMITTER PARAMETERS

	TRANSMITTER POWER (watts)	VOLTAGE V p-p	VOLTAGE V rms	MOMENT A-T•m^2
A	105	224	80	0.6 to 1.1 x 10^6
B	13	79	28	2.3 to 3.8 x 10^5
C	0.12	7.5	2.7	2.2 to 3.6 x 10^4
D	0.07	5.6	1	1.6 to 2.7 x 10^4

tunnel. The measured levels of signal field strength at the center frequency around 90 Hz, made with a 2000-turn ferrite core search coil and an HP302 spectrum analyzer, agreed reasonably well with the calculated fields as shown in Table 3.3-2. Consistent canister response was obtained with transmitting antenna drive voltages down to less than 5.6 V p-p which corresponds to a signal field of less than 64 μA/m rms at the receiver. It was observed that the downhole receiver notch and bandpass filtering was sufficient to permit operation in the presence of vertically polarized power line noise fields comparable in value to the transmitted signal. (Horizontally polarized noise fields could be significantly higher than the signal.)

TABLE 3.3-2

SIGNAL FIELD STRENGTH COMPARISONS
Vertical field in the tunnel ($r \approx 396$ m, $f_0 \approx 90$ Hz)
(μA/m rms)

CASE	CALCULATED H_v	MEASURED H_v
A	1450 - 2660	1550
B	550 - 920	570
D	38 - 64	-

After all downhole units had been emplaced at their final depths, it was determined that a tra. mitter drive voltage of 7.5 V p-p to the surface loop antenna provided consistently reliable operation under all conditions. Although it was not feasible to make signal or noise measurements at the final downhole receiver locations, estimates of signal strength are shown in Table 3-3.3.

TABLE 3.3-3

THEORETICAL DOWNLINK SIGNAL STRENGTHS

UNIT	RANGE (m)	H_v (μA/m rms)
210'	535	19 to 31
300'	518	21 to 35
400'	460	31 to 52

Since there was not any power in the tunnel for post-shot operations, downlink reception was only limited by attenuated atmospheric and internal noise. For the depth and conductivity encountered in the 210' hole, atmospheric noise at about 5×10^{-8} A/m$\sqrt{\text{Hz}}$ should predominate. In the receiver bandwidth of about 40 Hz, this would produce a total noise level of about 0.3 μA/m, or signal-to-noise ratios of 36 to 40 dB at each canister.

4. MECHANICAL DESIGN

4.1 DESIGN CONSIDERATIONS

The mechanical design of the telemetry electronics canister and antenna was set by DNA's prediction[12] of the worst-case free-field shock and pressure expected at the installation radius as shown in Table 4.1-1. These predictions were based on saturated tuff, but the final emplacement was in quartzite. Therefore, the final location radius was chosen to ensure that design performance limits would not be exceeded.

TABLE 4.1-1

MECHANICAL DESIGN ENVIRONMENT PARAMETERS

Axial Pressure	1 kilobar (10^5 kPa)
Lateral Pressure	0.76 kilobar (7.6 x 10^4kPa)
Velocity	125 fps (38 m/s)
Peak Acceleration	3000 G
Velocity Rise Time	2588 μs
Displacement	6.7 feet (2.04 m)

In order to meet system performance objectives in this environment, an 11-inch (27.94 cm) maximum diameter package for installation in a 14-inch (35.56 cm) minimum diameter borehole was evolved as shown in Figure 4.1-1. Segmented steel canisters, containing the electronics, were chosen in order to provide bulkheads for axial and radial support as well as assembly convenience. Electronics canister sections and module lengths are constrained by shock loads. The iron-cored solenoid antenna is potted within a fiberglass tube and is basically a solid structure. All sections are joined by 11-inch diameter (27.94 cm) alloy steel clamp bands. Although the clamp joint has a higher first cost than radial pin joints or flanges, it is far more convenient for assembly. The clamp joint is designed to preload the canister contents to help prevent internal connector separation under shock loads.

At low pressure levels (several hundreds of psi), the choice of stemming material (i.e., sand, grout, etc.) can effect a significant reduction in the pressure applied to the surface of the canister as compared to the free-

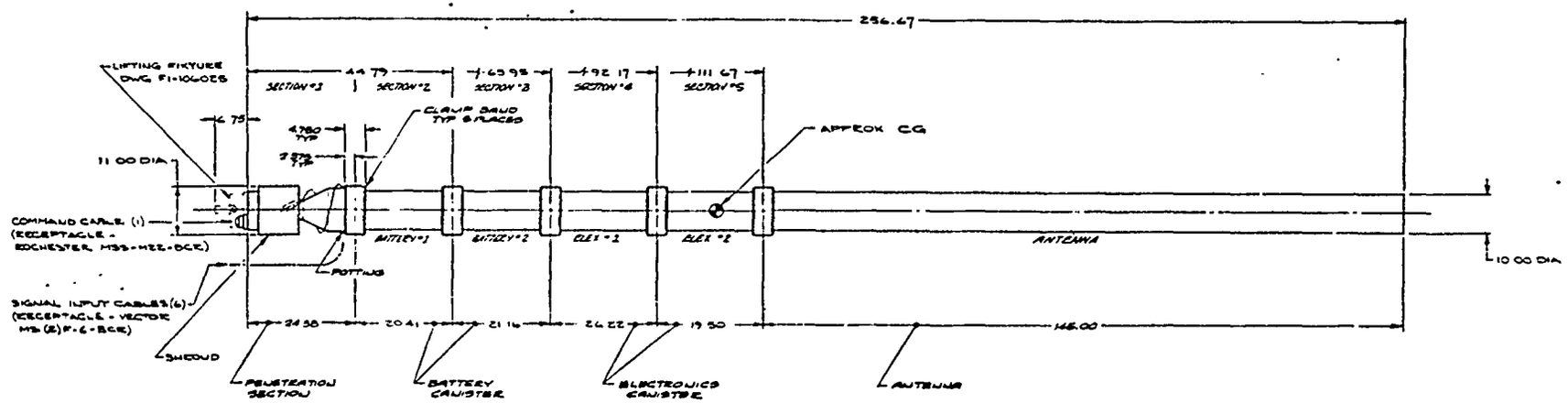


FIGURE 4.1-1

OUTLINE, TELEMETRY SYSTEM ELECTRONICS CANISTER AND ANTENNA

field pressure. However, at higher free-field pressures, this attenuation is reduced since potential stemming materials will rapidly compact. Therefore, it was assumed the canister surface would see free-field pressure. Alloy steel (e.g., HF4137) tubing, 9 inches (22.86 cm) in outside diameter by 1-inch (2.54 cm) thick, was used as the basic high pressure (1 kilobar or 10^5 kPa) structural containment for the electronics and is the preferred choice. The use of low carbon steel seamless pipe with an additional 1-inch (2.54 cm) fiberglass wrap is considered a viable alternative at the 1-kilobar level when alloy steel cannot be obtained. Low carbon steel pipe could be used alone at free-field pressures of less than 1/2 kilobar (5×10^4 kPa). Note that a 3-kilobar (3×10^5 kPa) environment could be withstood by an 11-inch (27.9 cm) diameter alloy steel pipe with a 2-inch (5 cm) wall, with a yield strength of 150,000 psi (1.03×10^6 kPa), assuming no increase in peak shock levels, but at proportionately higher cost.

The canister design is inherently long (approximately 20 feet or 6 meters) and narrow (9 to 11 inches or 23 to 28 cm). The question of canister orientation with respect to the source relates to the problem of joint strength. The expected high level for axial shock precluded the use of one or more articulated joints since such mechanical joints cannot be made, in a practical sense, with adequate tensile capability. Similarly, a design involving several distinct canisters connected by high strength cabling was rejected because of the added cost of a system with a multiplicity of penetration sections. (But the potential use of several canisters connected by cabling is feasible and might well be reconsidered for future designs involving much higher levels of free-field pressure and shock.) Consequently, it was decided to design a single, long integral structure with fixed joints to be oriented in a mostly radial direction. That is, joint strengths will be suitable for worst-case bending-mode responses with the canister installed at an off-radial angle of less than 30° and subjected to side loads of less than one third of the end load. However, these figures are based on very conservative design estimates and it is probable the canister can actually withstand considerably higher side loadings.

Initially, a "super lean" grout was the preferred choice for stemming material because it will accelerate the canister with well distributed and low surface shear loads. This is particularly important in regard to the

shearing action on electrical cables and ultimate clamp band joint yield caused by differential forces due to the antenna being lighter than the main canister. Also, installation was originally considered to be in tuff of density 2.0, so the lower grout density (1.7) would offset the greater canister density (2.0 to 3.0). Thus, the combination of the heavier canister and the lighter grout would tend to improve the density match between the canister and the free field tuff and lessen the probability for failing cable penetrations into the canister. However, the final installation was in quartzite (density approximately 2.6) and a rock matching grout was used for other reasons. This did not cause any obvious cable failures (although there is no way to be sure because of the lack of gauge data in the 210' and 400' units - see Section 5) and certainly did not cause any antenna joint failures, possibly because the match between the canister and quartzite is reasonably good.

4.2 DESIGN DESCRIPTION

The canister assembly consists of battery and electronics components installed in 9-inch (23 cm) OD alloy steel pipe sections. An iron-cored solenoid antenna structure contained within a heavy wall fiberglass tube of appropriate matching external diameter attaches to the end of the canister. There are five major sections to the canister: a cable penetration and EMP filtering section; two battery sections with electrical feedthrough harnesses; and two electronics sections with two separate modules each. The canister and antenna sections are connected by six fixed joints to form an overall length of about 20 feet (6 meters not including the lifting fixture). Periodic bulkheads are included as part of the modules inside of the canister to maintain pipe circularity, to conduct heat into the steel canister wall (which also serves as a heat sink) and provide a stiff mounting surface for the intermodule electrical connections. The modular subassemblies are keyed for fixed referenced interconnection patterns so blind connections are possible.

The basic design objective was to achieve an extremely stiff, relatively light internal construction that would minimize shock response deflection at the connectors. Loss of electrical contact because of shock load induced connector separation was a primary design problem. Miniature Amphenol MDM series connectors were used because of the proven performance of their "twist pin" design under high shock conditions, but are limited to an effective engagement distance of about 1/16 inch (1.6 mm). Thus, 1-1/2 inch (3.8 cm) thick alloy steel bulkheads are captured between canister sections (at the clamp bands) at about 24-inch (61-cm) intervals to support the module loads with minimum deflection. All other bulkheads are either 1-1/8 inch (2.86 cm) carbon steel (batteries) or 7075-T651 aluminum (electronics) to suit stiffness and weight requirements. Aluminum structural support elements (battery containment wafers and electronics spacer rings) are used for stiffness and lightness. The heavier battery modules are limited to an overall length of about 21-1/8 inches (54 cm) and are preloaded to 150,000 pounds (667,200 newtons) by 12 half-inch (1.27 cm) alloy steel bolts. Individual electronic modules are limited to about 14 inches (36 cm) because only five half-inch bolts are used to provide a preload of 62,500 pounds (278,000 newtons) and each bolt may experience greater relative forces

during shock. However, any two electronics modules are limited to an overall length of about 26-1/4 inches (67 cm) per section, i.e., per captured support bulkhead. The end module of each canister is shimmed prior to being joined to the next adjacent canister, so that the clamp bands cause additional preloading to the entire system when bolted solid.

4.2.1 Penetration Section

The penetration section, Figure 4.2-1, makes use of rugged high pressure underwater type connectors and is designed to provide maximum protection for the input signal lines. The 1-1/8 inch (2.86 cm) tapped hole (7UNC-28 thread) in the end plate is provided for mounting the system lifting fixture. There is a command and checkout connector, used prior to the shot, which need not survive, that is attached directly to this exposed face. The six incoming signal (gauge) connectors are protected from relative displacement between the canister and the free-field media by the cyclindrical shield sleeve. The incoming electrical cabling wraps about the canister such that significant relative motion between the canister and the free-field media will not create high cable tension or shear where the cabling enters the connectors. The external cabling is intended to be loosely wound with a helical diameter that becomes greater than that of the clamp band as it proceeds from the surface of the housing and turns back into the free-field media.

The stiff, alloy-steel end plate bolted to the left end of the penetration section alloy steel housing is deflection limited to preclude any possibility of an external pressure-induced collapse mode that might pinch the electrical leads as they proceed from the incoming connectors and turn into the center of the housing. The electrical leads inside the penetration housing are potted as they wind about the inside surface and attach to the EMP filter can baseplate. The baseplate is designed to flex axially and maintain contact with the housing potting material so it will not load the connection where the incoming leads enter the filter can assembly. The axial deflection of the right-hand connector bulkhead of the filter can assembly will be less than one fourth the magnitude of allowable separation for the MDM pin connector pair that joins the penetration section to the battery section.

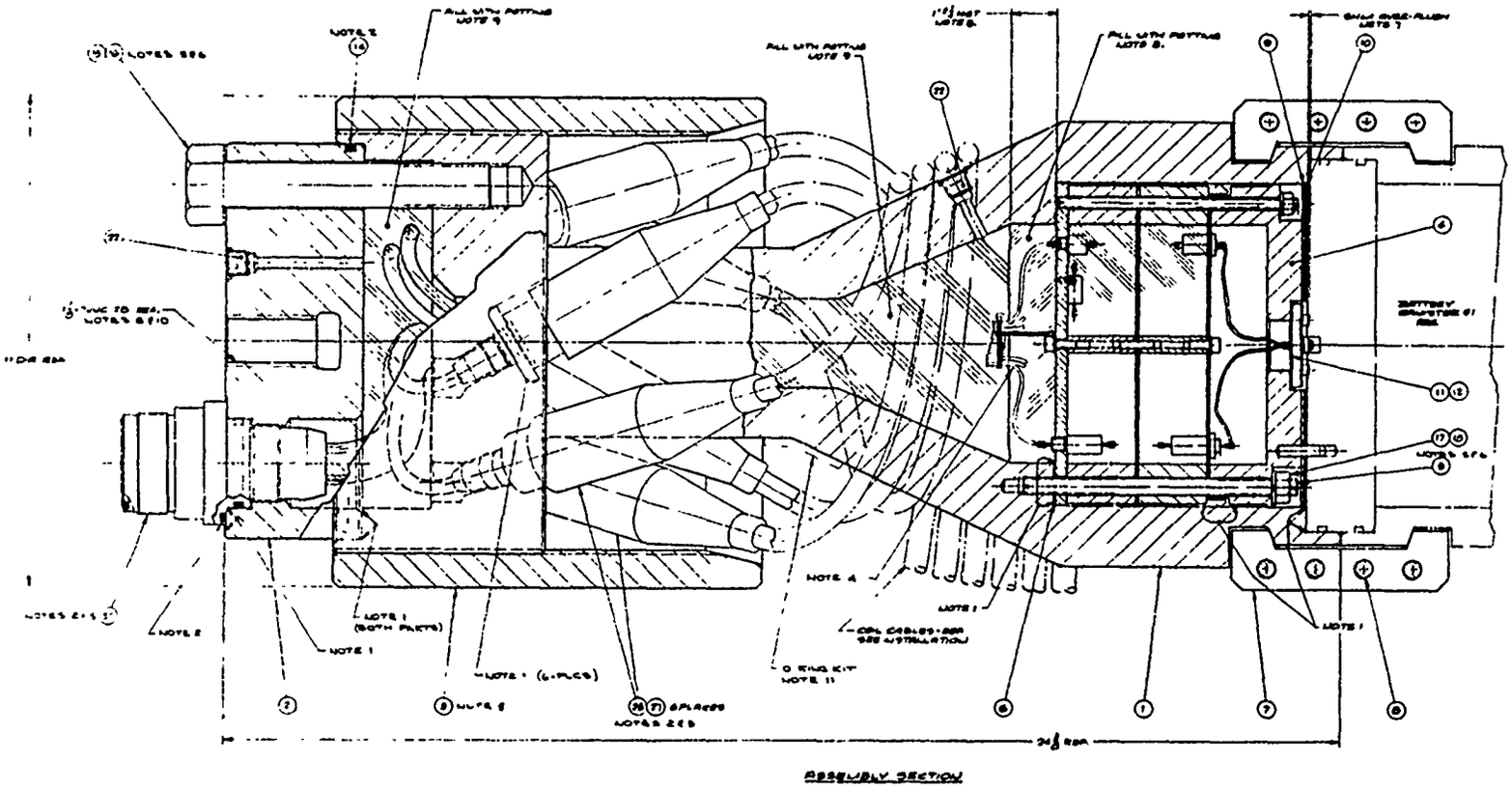


FIGURE 4.2-1

PENETRATION SECTION LAYOUT

4.2.2 Battery Sections

There are two battery sections, Figure 4.2-2, containing six aluminum wafers or spiders with a total of 48 potted button cell battery arrays, i.e., 8 battery arrays per spider. Each battery is potted in the wafer with a silicone rubber compound (Sylgard 184). In each section, three spiders are joined in an assembly preloaded by 12 high-strength half-inch studs. The length of a battery section is about 21 inches (53 cm). Electrical cabling from the penetration section passes through the battery sections in a potted helical winding inside a central G-10 Fiberglass tube. Battery spiders are separated from each other by an intermediate steel bulkhead sandwiched between two G-10 Fiberglass spacers. The purpose of the intermediate bulkhead is to maintain a circular mode shape for containment tube deflection. The outside diameter of the battery section spiders is less than the inside diameter of the containment tube so there is no way for containment tube distortion to pressurize and damage the potted arrays of button batteries.

4.2.3 Electronics Sections

There are two electronics sections, Figure 4.2-3, each containing two modules of stacked electronics PC board wafers interconnected by a wire cage around the periphery of each module, Figure 4.2-4. Board-to-board wiring is accomplished by inserting wires (0.024 inch or 0.6 mm diameter half hard drawn berylium copper) of appropriate length in up to 100 individual spring type pin sockets (Amphenol P/N 3-331272-5) around the periphery of each board. The wire ends are crimped to prevent axial motion during shock. Amphenol MDM twist pin series connectors carry the stack wiring from module to module, through bulkheads that restrain motion of the stacks in the canister. Each electronics section uses the same connector pattern with the direct plug-in MDM connectors. Proper canister/connector alignment is maintained by a referenced system of dowels. Each wafer stack is preloaded by five high-strength half-inch studs. Individual module lengths are limited to about 14 inches (36 cm) and overall section lengths are limited to about 26 inches (66 cm). The general configuration of an electronics module is similar to that developed on a smaller scale at Sandia Laboratories, Albuquerque, New Mexico, to telemeter data from a 155-mm shell.

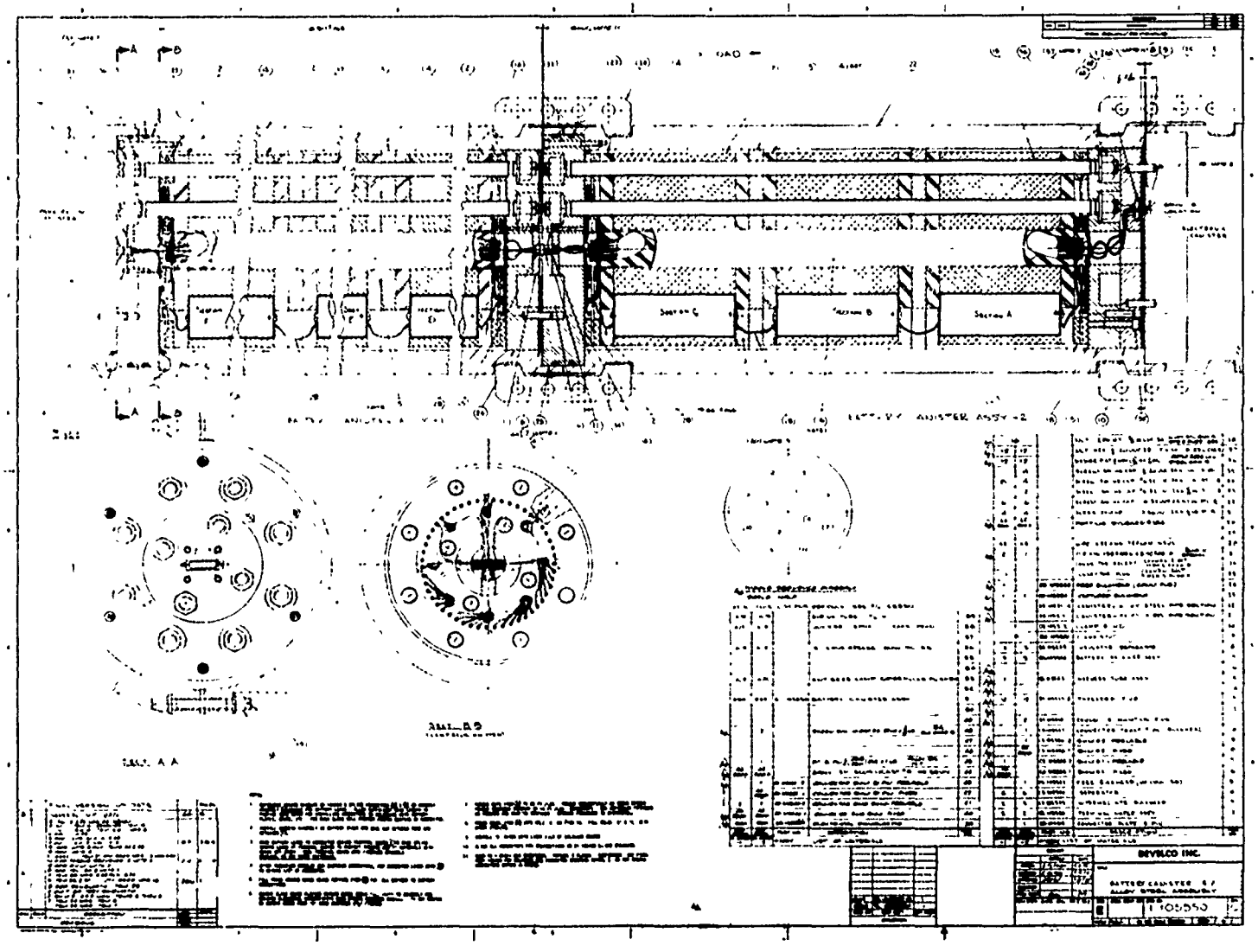


FIGURE 4.2-2

BATTERY SECTION LAYOUT

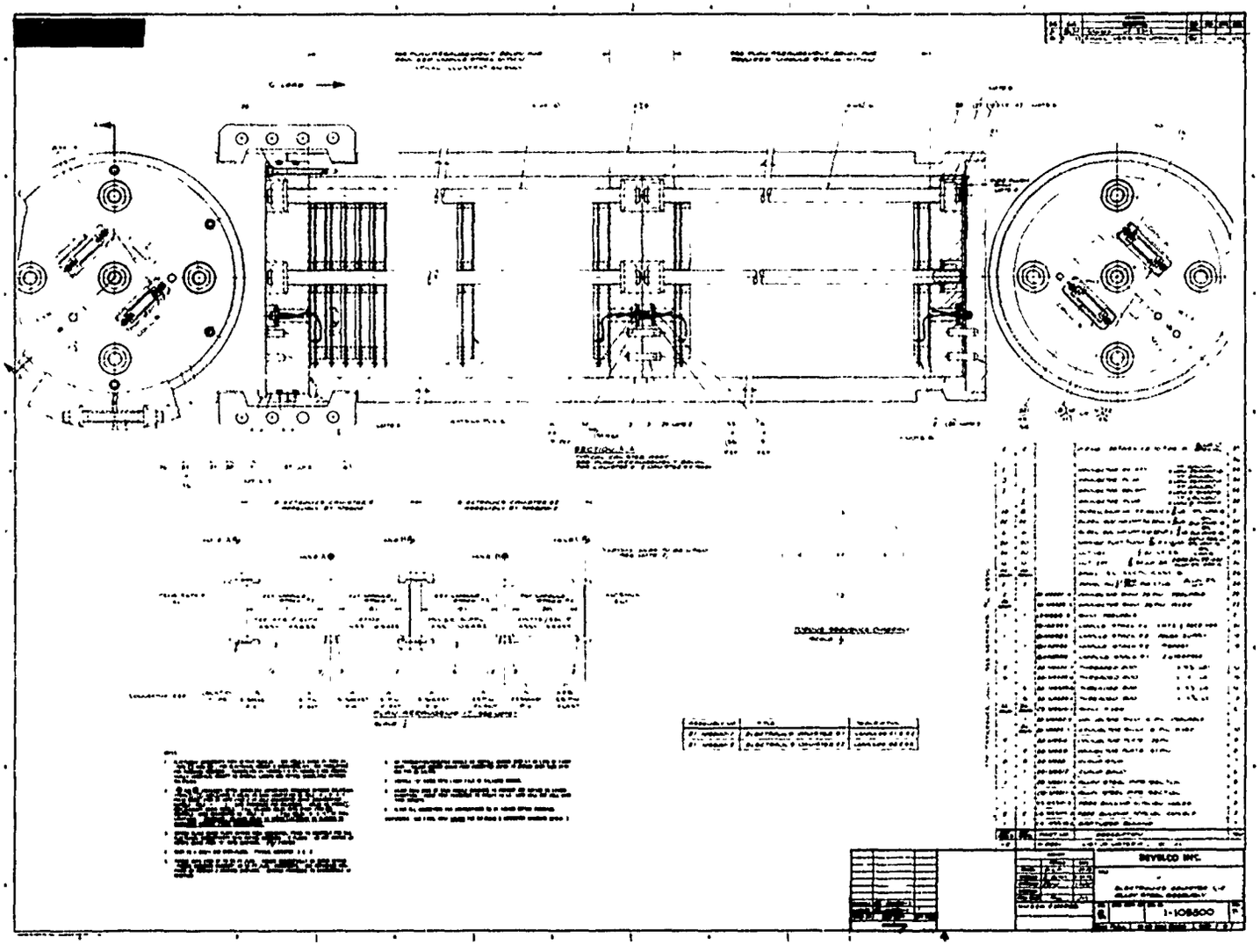


FIGURE 4.2-3

ELECTRONICS SECTION LAYOUT

Each wafer, Figure 4.2-5, within an electronics module subassembly consists of a circuit board, sandwiched between two bonded thin (0.015 inch or 0.4 mm) G-10 Fiberglass insulating rings, which is in turn sandwiched between two bonded structural aluminum rings. Standard electronic components, including hybrid circuits, standard IC's, transistors, diodes, carbon and metal film resistors, ferrite and tape core coils, capacitors, etc., were successfully used without problems. The only constraints were: unknown types (e.g., hybrid devices) were type shock tested; RCA ceramic package IC's with round lids were not used because of reported package weakness at high shock; and capacitor usage was limited to ceramic CKO and solid tantalum types because of previous user experience at high shock levels. The only special precautions taken at assembly were to insure each device was adequately supported by the PC board, a shim or potting material, and to solder all feedthroughs. Components are conformal coated, both sides of the PC board are potted with 14-lb/cu ft (224 kg/m^3) urethane foam, then each wafer is faced off to exact height prior to stacking in the module. Electronic components that generate significant heat for a short time are protected by aluminum bars bonded to the components or plates for component mounting to provide local thermal mass. These bars are in turn thermally connected to sheet aluminum thermal sink wafers sandwiched in between the electronics wafers. Ultimately, generated heat conducts through the stacked wafers to the module bulkheads and into the heavy containment canister wall. Note that the aluminum support rings on the wafer greatly aid this conduction process.

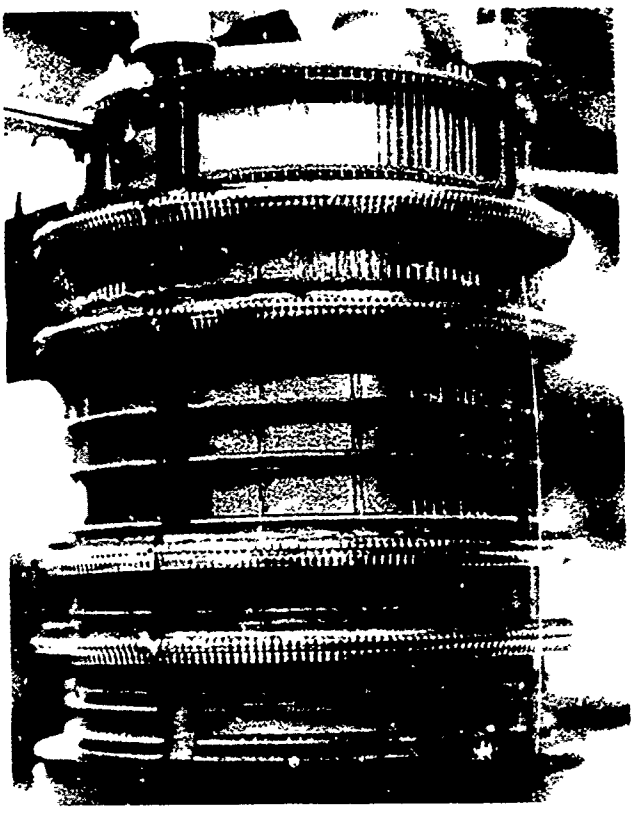


FIGURE 4.2-4
ELECTRONIC WAFER STACK

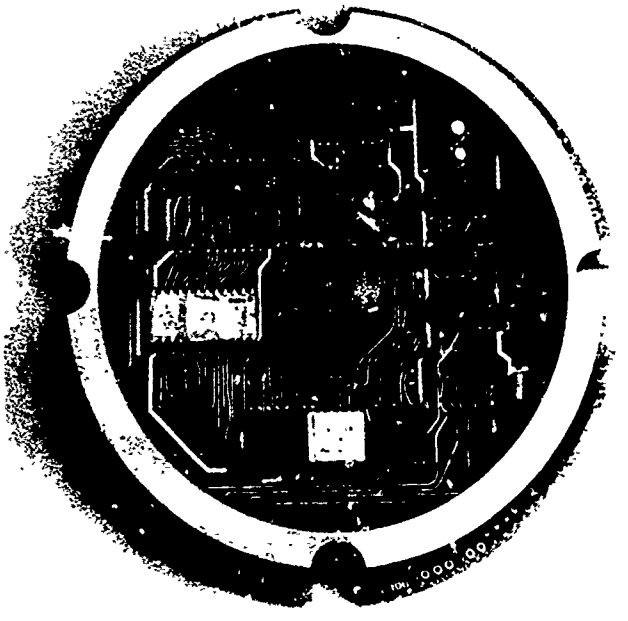


FIGURE 4.2-5
PC BOARD WAFER

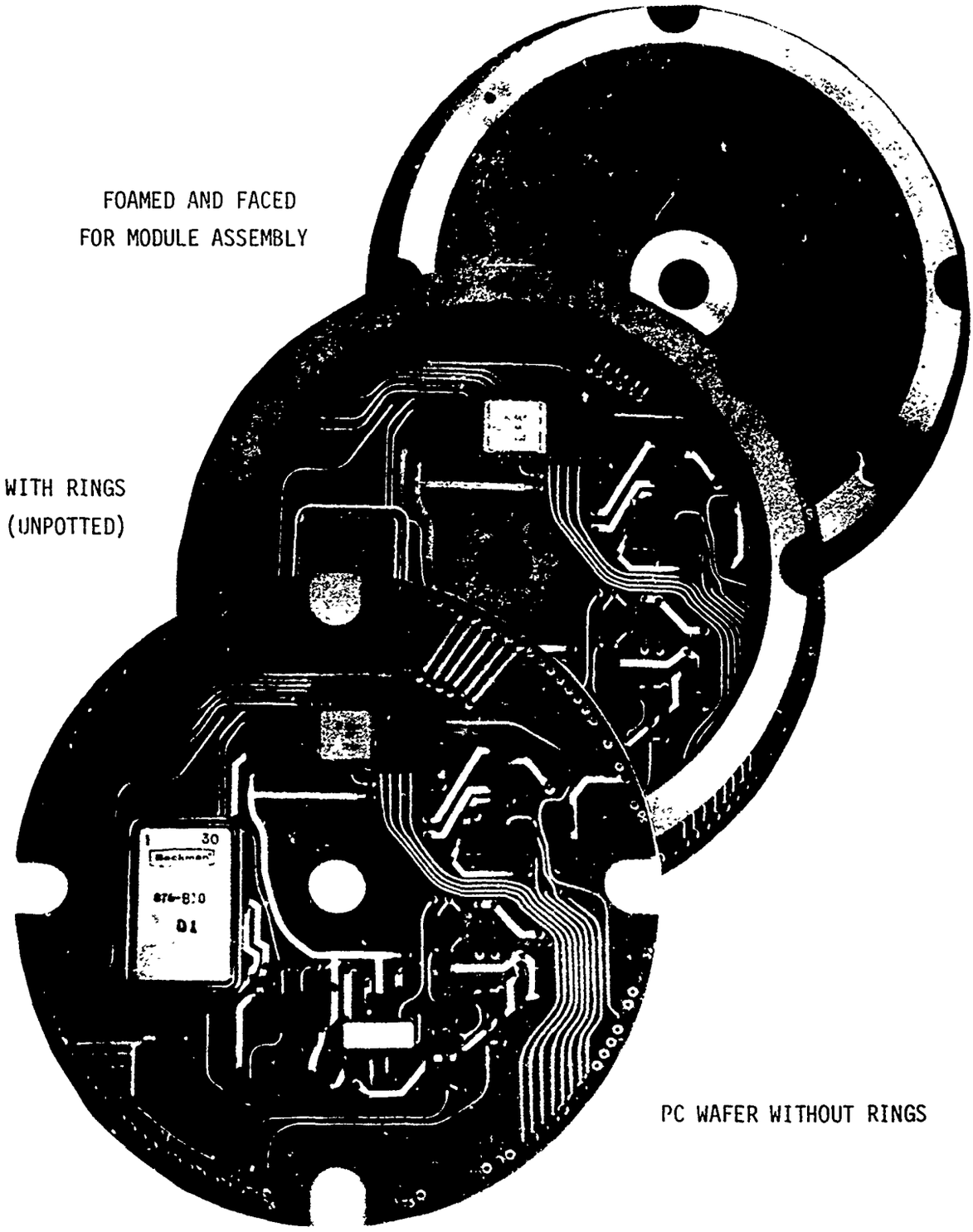


FIGURE 4.2-6

PC BOARD WAFER, SHOWING STAGES OF CONSTRUCTION

4.2.4 Antenna Assembly

The antenna, Figure 4.2-7, is made up of three nested subassemblies: the core, the coil, and the containment tube.

The core consists of 100 pounds (45 kg) of many long (120" or 3 m), narrow (2" or 5 cm), thin (0.006" or 0.2 mm) electrical steel laminations epoxy potted inside a 3-1/2-inch (8.89 cm) outside diameter G-10 Fiberglass tube. This tubular core assembly is supported by stiff syntactic foam pads at each end and by potting material with low shear characteristics along the outside diameter cylindrical surface. When subjected to shock loading, the core assembly is expected to displace relative to the coil assembly and will dissipate energy in shearing the potting material in the annulus between the core and coil and in crushing the syntactic foam pad at the base.

The coil is a bifilar winding of #10 magnet wire making 164 turns about a supporting G-10 tube. Axially, the turns are insulated by an associated spacer winding of 1/8 inch (0.32 cm) diameter polyethylene rod. Radially the turns are insulated from the return leads by a multilayer wrap of polyester-impregnated 1581 fiberglass cloth. Return leads are then wrapped in fiberglass. Axial EMP shielding screen strips are then located and wrapped on top of the coil. The annulus between the coil and the core is potted with Sylgard 184. The annulus between the coil and the containment tube is epoxy potted.

The containment tube is an epoxy-impregnated fiberglass structure wrapped with 1581 fiberglass cloth, with 10-inch (25 cm) OD and a 6-inch (15 cm) ID. The wrapping captures an alloy steel clamp band collar with a very strong shear bond at the end where it attaches to the electronics canister. The thick captured bulkhead is designed for very small axial shock load deflection and also to help maintain the heavy axial preload in the attached electronic and battery canisters. The electrical leads from the coil to the connector in the captured bulkhead and also the screen strip leads to ground are fully potted in the final assembly.

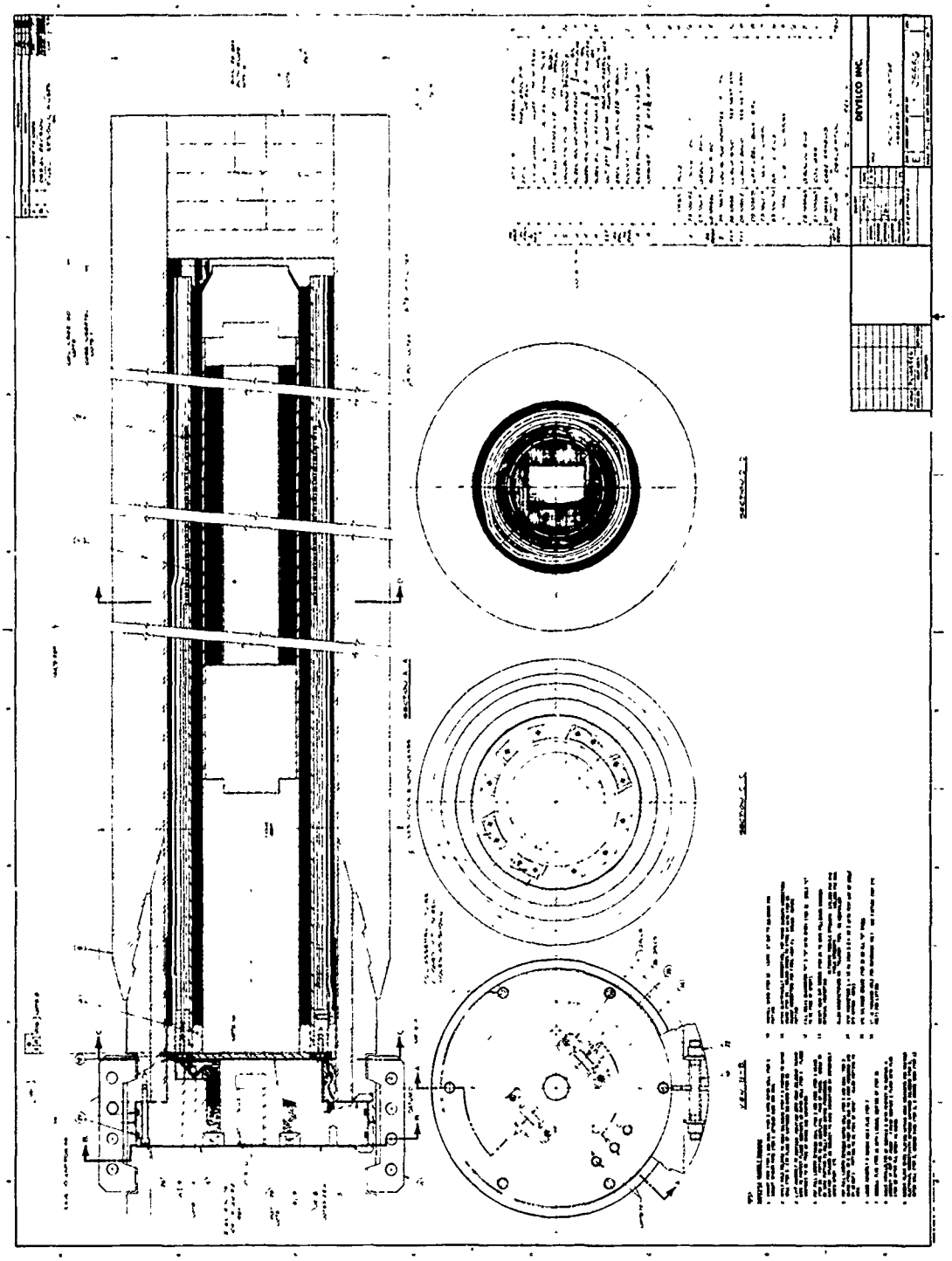


FIGURE 4.2-7
ANTENNA ASSEMBLY

4.3 DESIGN MARGINS

Refer to Table 4.1-1 in which the free-field mechanical design environment is stated, and to Table 4.3-1 which summarizes the capability and estimated response of the final design. The axial pressure is expected to be 1 kilobar (10^5 kPa), the lateral pressure is expected to be 0.76 kilobar (7.6×10^4 kPa). Containment tube collapse results from lateral pressure. The best reference[8] on the capability of the tube to resist external lateral pressure indicates that the alloy steel tube is good for a minimum of 1.19 kilobar (1.19×10^5 kPa). Therefore, pressure containment design margin is $(\frac{1.19}{0.76} - 1) \times 100 = 57\%$.

TABLE 4.3-1
LOAD SUMMARY

DESIGN CAPABILITY

Pressure	1.10 kbar (1.19×10^5 kPa)
Axial Shock (tight assembly)	>4000 G

	Friction Coeff.	Maximum Load
Clamp Joint Tension	0.3	1,581,000 lbs (7.1×10^6 N)
	0.25	944,230 lbs (4.25×10^6 N)
Clamp Joint Moment (approximately 2 times tension capability in in-lbs)	0.3	3.1×10^6 in-lbs (0.35×10^6 N·m)
	0.25	1.9×10^6 in-lbs (0.21×10^6 N·m)
Clamp Joint Shear	-	626,000 lbs (2.8×10^6 N)

ESTIMATED DESIGN RESPONSE (for expected environment)

Joint Tension	787,000 to 1,188,4000 lbs (3.54 to 5.35×10^6N)
First Bending Mode Moment	97,835 in-lbs (11,045 N·m)
Relative Axial Translation of antenna core	2.5 inches (6.35 cm)
Internal Tie Bolt Preload Stress	160,000 psi (1,102,400 kPa)

*All tension figures are for yielding failure in bolts and may or may not represent actual system failure; i.e., there is probably additional margin.

The peak acceleration expected is about 3000 G and the velocity rise time is about 2588 microseconds. Canister orientation is such that the lateral shock will be about one third as intense as the axial shock. The MDM pin connectors that maintain electrical contact between internal canister module subassemblies can separate up to 0.157 cm before electrical contact is destroyed. Consider a 2-foot (61 cm) long electronics canister. Axial loading results in a canister length relative deflection of 40 mils (0.101 cm). Lateral flexing of the system is estimated to increase this by 15 mils (0.038 cm). In addition, the mechanical installation tolerance amounts to a separation of 15 mils (0.38 cm), for a total of 70 mils (0.177 cm). Against this buildup, the upstream male connector "floats" 20 mils (0.5 mm) and the clamp band preloads the two module electronics canister stack by a minimum of 30 mils (0.76 mm). Design margin is $(\frac{112}{70} - 1) \times 100 = 60\%$. Based upon elastic buckling, the G-load design margin of the half hard berylium copper wire cage about the electronics modules calculates to be 106%. The maximum unsupported length of connector lead is 1.5 inches (3.81 cm). The connector lead G-load design margin is measured to be in excess of 100%.

The estimated tensile strength of the clamp joint at the antenna is a function of the assumed level of friction in the clamp joint at the time of the shock. If the effective friction coefficient is 0.3, the design margin will be between 33% and 100% depending upon loading assumptions. An increase in friction level rapidly improves design margin and vice versa. At the time of assembly clamp band friction is reduced by a light inert lubricant to ease the problem of inducing preload by torquing the clamp band studs. The very high clamping pressure will squeeze out the lubricant and friction will then increase.

The total free-field velocity shock is 125 fps (38 m/s). The antenna core is supported by shock pressurized Sylgard 184 potting along the sides of the core tube with a shear strength of 93 psi (641 kPa), and by the crushable (12000-8000 psi) syntactic foam pad at the bottom. The calculated relative axial motion of the core corresponding to this magnitude velocity shock is 2.5 inches (6.35 cm). The antenna assembly allows a relative motion of 7 inches (17.78 cm) before the end of the core iron penetrates inside the metal clamping collar that supports the fiberglass antenna containment tube. Thus the calculated antenna core motion design margin is 180%.

The antenna design involves solidly wrapped and potted electrical components. The core assembly is potted inside the coil tube which in turn is potted inside the structural containment tube. At least two layers of polyester and/or epoxy resin impregnated 1581 glass cloth separate the layers of electrical circuitry. No short circuit mechanism seems to be present in the design. The subcontracted fabrication has been closely monitored and all significant electrical assemblies have been directly supervised by Develco personnel. The external pressure design margin of an empty fiberglass containment tube is estimated at 25%. The design margin of the filled and potted tube will be larger. Even if the containment tube should crack or collapse, no mechanism for electrical failure is apparent, so long as the coil subassembly does not fracture.

There are three aspects to penetration section design margin. First, the cabling and connectors attaching on the outside are configured to allow significant relative motion between the free-field medium and canister without introducing excessive cable shear or tension at the cable entry points. The connectors are protected by a heavy cylindrical guard. Second, the penetration canister deflection is calculated to be small in the end plate region to preclude any squeezing or pinching of the internal cabling. In the neckdown section, the penetration section will yield and bend, the yielding and bending strain energy capacity of the neckdown section is several times the relative kinetic energy of the penetration section dynamic mass, calculated for a velocity shock of 125 fps (38 m/s). Third, the potted cable leads inside the penetration housing will slump with the potting material and bend with the housing.

The base plate of the filter can assembly to which the incoming cabling attaches is designed to deflect as much as the potting material slumps to preclude differential loading of the incoming cable leads.

To further protect against possible incoming cable connection failure, a soft, low shear potting material is used adjacent to the filter can base plate. The remainder of the penetration canister housing is filled with hard pot material.

Overall, so far as the foreseen design problems are concerned, the mechanical design margin of the canister and antenna assembly is estimated at 50%, i.e., an assembly installed in a free-field region 50% more severe than the design free-field region would be likely to perform in a satisfactory manner without electrical fault induced by mechanical failure.

4.4 SHOCK TESTING

Three kinds of pre-shot mechanical testing were conducted on this program:

A. Qualification shock testing of electronic and battery component types at 3000-4000 G levels.

B. Mechanical design verification test of an assembled and operating prototype test module (containing typical battery wafers, power supply and MPU/memory functions) which was subjected to a shock over test in excess of 3000 G (all components operated through the highest level shock pulse but a failure occurred when the 72 V main power buss shorted to the low voltage busses after the main impulse - this was later found to be due to a sliver of metal trapped in the connector during its manufacture, a common happening which responded to cleaning procedures).

C. Shock all final system production PC boards (non-operating but stacked in equivalent module height for efficiency) at 3000 G prior to final testing and assembly in the system. (There were no failures due to shock and this was discontinued after the PC boards for the first two and some of the third system had been done.)

The facilities at Sandia Laboratories, Albuquerque, New Mexico, were used for the prototype module and PC board test because of the weights and shock levels involved.

Full scale tests on an entire canister/antenna assembly using Sandia drop towers, rocket driven cable, or rocket driven sled facilities were seriously considered, but rejected for reasons of cost and because it is not possible to reasonably duplicate the expected distributed surface shear loads that will be applied to the assembly when it is subjected to the underground shot. Other verification tests were considered and rejected. These involved test sections buried near a large underground charge of high explosive and/or a helicopter drop test also involving a timed H.E. reaction to provide simultaneous shock and pressure. It is very difficult to fairly simulate the environment produced by an underground nuclear explosion without having an underground nuclear explosion.

5. RESULTS

Three Develco Underground Telemetry Systems were installed as part of the Waterways Experiment Station (WES) Interface Experiment on the Mighty Epic event, 12 May 1976. The experiment, which was fielded and operated by WES, consisted of velocity, acceleration and stress measurements above and below an interface between tuff and quartzite regions. In general, gauges located above the interface were wired to and powered from the surface via special hardened cables, and gauges located below the interface were connected to the battery powered telemetry canisters although there was some overlap at the interface zone. A typical connection between the telemetry system and the WES signal cable junction box is illustrated in Figure 5-1 . The stress gauge and telemetry command cables that were routed outside the hardened conduit are shown while the other signal functions were connected to gauge canisters via the conduit that is not yet in place. Develco supplied technical support for the data dump operations conducted 13 to 17 May 1976 when complete chart and magnetic tape recordings of the memory contents were obtained for analysis. Also, follow up operations were conducted on 10 and 11 June 1976 to check the operating condition of the three systems, verify system battery capacity (See Section 2.5) and measure transmission parameters (See Section 3.2). Since the details of the experiment and subsequent data analysis will be published by WES only the general results known at this time are discussed in the following.

All three downhole systems responded perfectly to the transmitted downlink commands at frequencies and signal levels comparable to pre-shot performance during both the May and June operations. Initially, an attempt was made to interrogate the canisters and channels in order of priority but this proved very cumbersome and was largely disregarded as soon as it was determined there were no abnormalities in the canister current drains. The parity error rate on uplink transmissions was relatively low ($\approx 10^{-5}$); there was only one instance of loss of synchronization during a long dump (Channel 1, 210' unit) and it was easily re-synchronized with the receiver controls. However, as a consequence, most later dumps were limited to 48 blocks but this was probably too conservative. There were very few instances when it was necessary to repeat the interrogate commands because the downhole system failed to respond. (When it happened, it was usually after a unit had been operating for some time and may

FIGURE 5-7

TYPICAL CONNECTOR BETWEEN THE TELEMETRY SYSTEM AND THE WES SIGNAL CABLE JUNCTION BOX.

have been caused by temperature or voltage changes as well as electrical noise since in each case the unit would respond after resting.

During the May operations, it was observed that the 300-foot canister memory stored valid ground motion data, including significant late time information, on all 11 operating channels. (Channel 1A was connected to a gauge known to have failed before the shot.) However, two of the stress gauges, which were connected to the canisters by exposed (not hardened) cables, appear to have failed during shock but only after the amplitude peak occurred. A typical velocity gauge output is shown in Figure 5-2 where the amplitude is given in terms of the stored digital number.. After applying the appropriate calibration factors the data arrival times, amplitudes and signatures were appropriate to the gauge types and their location in all cases, it is believed. The correct arrival times and the well behaved data records confirm that this unit received the proper Ready and FIDU data acquisition commands.

However, the 210' and 400' units did not contain any recognizable signals and the memory information looked like offsets or (near) zeros depending on the canister and channel. It is extremely unlikely that the lack of earth motion data in these units was caused by a malfunction within the telemetry canisters themselves. First, much of the same circuitry (microprocessors, timing, power supplies, etc.) that controls the acquisition function is also required for the transmit function and performance was consistent and reliable before and after the shot. Second, the ability to lock out external commands for 30 seconds during an acquisition cycle precludes an outside cause during that time, e.g., due to EMI/ECI interference). But if an internal glitch occurred during shock (e.g., in the MPU or power supplies), it would cause the memories to store 0's, 1's or random data depending on the cause; this was not the case and there were distinct and consistent differences in the stored information between channels that appeared to be nearly normal for quiescent gauges. Finally, the fact that the data acquisition commands to each canister came from the same source, the command lines were (presumed to be) well shielded and the 300' unit did start acquisition at the correct time, suggests that there was

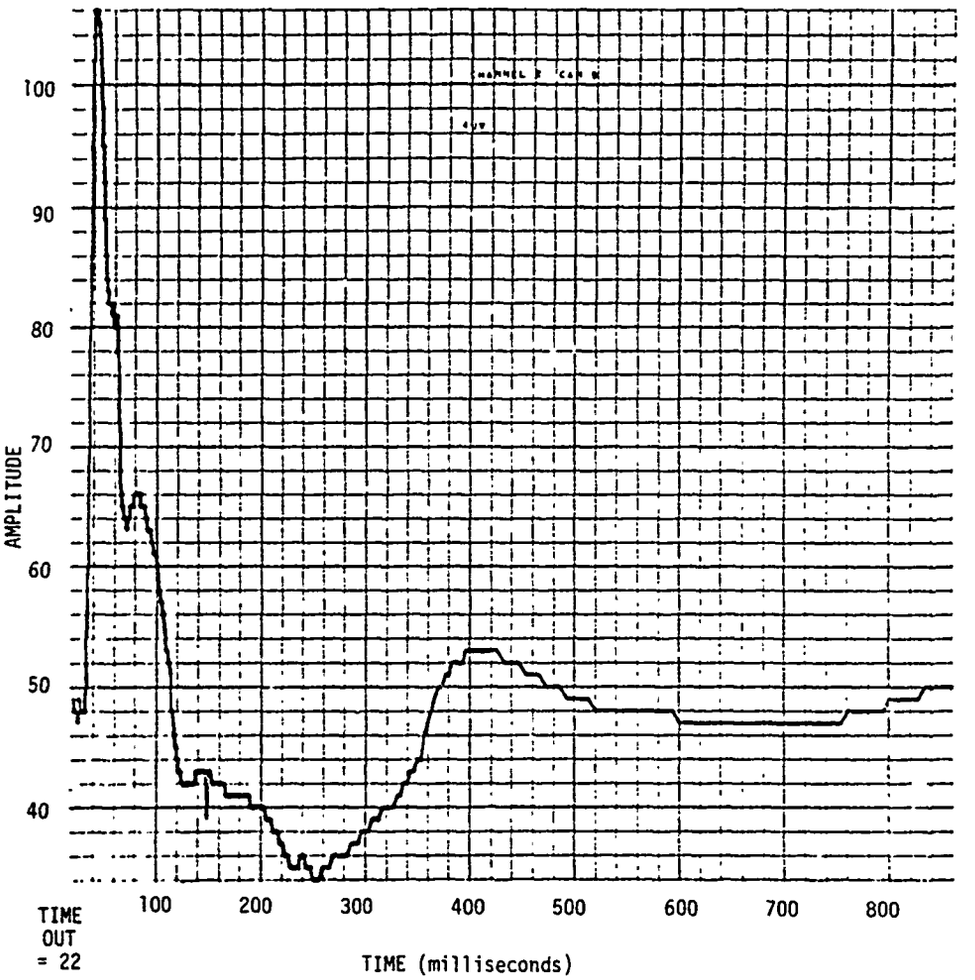


FIGURE 5-2

DATA FROM WES GAUGE #4UV (VERTICAL VELOCITY), CHANNEL 2B OF THE 300' CANISTER COMPUTER REDUCED FROM MAGNETIC TAPE RECORDING AND TRANSMITTED DIGITAL OUTPUT BY T.A. STOUGH AND R.A. SHUNK OF ELECTROMECHANICAL SYSTEMS, INC.

not any false pretriggering (e.g., by induction) and all units initially received correct commands.

The possibility of post shot false commands is much more likely based on the circumstantial evidence available. It is known that there were massive cable failures of both the unprotected command cables and the hardened WES signal cables at numerous locations that began within the first 100 ms. There was undoubtedly considerable cross shorting or at least resistive paths created among functions in all cables and there were supply voltages in other experiment cables that were not turned off until a considerable time later. Therefore, it seems most likely that the two canisters without data were triggered post shot by an undetermined source coupling almost directly to the command lines which caused these units to rewrite baseline data in their memories. This theory is given some credence by the fact that new and unique data (not ground motion) was found to have been recorded in the 300' canister memories between the May and June interrogations which was probably triggered in the same way be a severe electrical storm that reportedly occurred in the area during that period. Although simple command signal circuits were originally designed under the constraint that there would be no downhole voltages present post shot, it is obvious now that future systems should use complex coded signals to prevent any possibility of spurious signals retriggering the system.

It is estimated that the two closest-in canisters were exposed to an environment on the order of, and possibly in excess of, the 1 kilobar (10^4 kPa) and 2000 G design goal based on the WES preliminary analysis of hardwired gauge data. The farthest-out canister was, of course, exposed to somewhat lower levels, but all units appear to have been subjected to considerably higher side loadings than the design minimums. All available evidence suggests the telemetry canisters themselves worked properly in the data acquisition phase and survived the shocks in good working order. Further, there were no apparent changes in the downhole antenna tuning, as had been considered possible, since frequencies and power levels appeared to be about as they had been pre-shot. Thus, the Mighty Epic operation demonstrated that data storage and retrieval can be successfully accomplished under severe environmental conditions.

6. CONCLUSIONS AND RECOMMENDATIONS

Overall, the underground telemetry system development and its use on the Mighty Epic Interface Experiment has been a success. The ability to transmit data, by wireless means, from significant underground depths has been demonstrated beyond a doubt. The mechanical design concepts for protecting complex electronic systems from very severe mechanical shock environments have been proven. Also, previously unobtainable late-time motion data was recorded, in the 300' borehole, which is probably very important for the study of interface motion. However, the unfortunate loss of data from two of the units, probably from accidental post-shot retriggering, dramatically demonstrated that fault-causing conditions cannot be avoided under such complex conditions. Thus, it is recommended that future systems incorporate complex digital address codes to avoid retriggering as well as dedicate some system capacity to diagnostic information when problems do occur.

REFERENCES

1. Kimball, K.B., A Subterranean Radio Telemetry System for Earth Motion Data Acquisition, SC-DR-70-463, Sandia Laboratories, Albuquerque, NM, August 1970.

2. Smith, R.L., Field Report - Magnetic Communication Test at NTS, Report No. 818-721101-1, Develco, Inc., Sunnyvale, California, November 1972.

3. Smith, R.L., Test of Electromagnetic Communication Through the Earth, Report No. 823-721218-1, Develco, Inc. Sunnyvale, California, December 1972.

4. Rorden, L.H., and Bacon, L.C., A Subterranean Data Retrieval Concept, Technical Note 740411, Develco, Inc., Sunnyvale, California, April 1974.

5. Rorden, L.H., L.C. Bacon, R.L. Smith, T.C. Moore, and A. Weston, Underground Telemetry System Development - Design Definition Phase, Report No. 937-750107, Develco, Inc., Sunnyvale, California, July 1975.

6. Underground Telemetry System, Prototype Shock Test Report, Contract No. DNA001-74-C-0298, Report No. 937-750510, Develco, Inc., Sunnyvale, California, April 1975.

7. Ramo and Whinnery, Fields and Waves in Modern Radio, John Wiley & Sons, New York 1944, 1953.

8. Blake, A., "Formulas for Canister and Pipe Design in Underground Nuclear Emplacement", Journal of Pressure Vessel Technology, May 1974.

9. Rorden, L.H., A Study of Low-Noise Broadband VLF Receiving Techniques, AD660 050, Stanford Research Institute, Menlo Park, California, Sept. 1965.

10. Grover, F.W., Inductance Calculations: Working Formulas and Tables, Dover Publications, Inc., New York 1962.

11. Terman, F.E., Radio Engineers' Handbook, McGraw-Hill Book Company, Inc. 1943.

12 Ellis, Major H.B., Letter of 1/11/74, DNAFC-TD.

APPENDIX A

PRINTOUT OF COMPUTER PROGRAM

 DELIVERED JUN 3 0 1975

```
00010                          NAM    COMBA
00020                  * COMB.A  REV. JUNE 17, 1975
00050                  * NOTE: $CC IS USED FOR CONSTANTS NOT YET :=VALUE
00070       0000       TIMOUT EQU    $0000
00080       0018       ATOD   EQU    $18
00081       0018       DDRA   EQU    $18
00082       0019       CRA    EQU    $19
00083       001B       CRB    EQU    $1B
00084       001A       DDRB   EQU    $1A
00085       001A       PIRB   EQU    $1A
00086       000E       XON    EQU    $0E
00087       0002       XOFF   EQU    $02
00088       000A       PWROFF EQU    $0A
00090       0000       CANCHA EQU    $00
00091       0000       ONE    EQU    $00
00092       0008       ZERO   EQU    $08
00098 3E00                     ORG    $3E00
00099                  *   SET UP PIA
00100 3E00 4F                  CLR A
00110 3E01 97 1B               STA A  CRB      SELECT DDRB
00120 3E03 C6 1E               LDA B  #$1E   = 01 111 0
00125 3E05 D7 1A               STA B  DDRB
00130                  * "DDRA ALREADY IN INPUT STATE" -- E. HUTCHINS 1/3
00140 3E07 C6 25               LDA B  #$25
00150 3E09 D7 1B               STA B  CRB      SELECT PIR B
00155 3E0B D7 19               STA B  CRA      A
00160 3E0D D6 1A               LDA B  PIRB     GET DATA
00170 3E0F C5 80       POWER   BIT B  #$80
00180 3E11 27 4F               BEQ    OUTD
00190                  ***** TO XMTR PROC.
00250                  * INSERT REV.A
00251                  * PIRB BIGIT #4 LOW, HIGH
00260 3E13 7F 001A     AQUIRE  CLR    PIRB     LOW FOR SURE.
00270 3E16 86 10               LDA A  #$10
00280 3E18 97 1A               STA A  PIRB
00290                  *       END;  INSERT REV.A
00300 3E1A 8E 13FF             LDS    #$13FF
00310 3E1D FE 3FAF             LDX    TABL-2
00320 3E20 86 40               LDA A  #$40       c/o 0000
00330 3E22 95 1A       ED      BIT A  PIRB
00340 3E24 27 FC               BEQ    ED
00360 3E26 95 1A       WAITO   BIT A  PIRB
00370 3E28 02                  NOP
00380 3E29 09                  DEX
00390 3E2A 26 FA               BNE    WAITO
00400 3E2C CE 3F81     PANIC   LDX    #TAB
00410 3E2F 96 18               LDA A  ATOD
00420 3E31 E6 00               LDA B  X
00430 3E33 96 18       GROU1   LDA A  ATOD
00440 3E35 36                  PSH A
00450 3E36 5A                  DEC B
00460 3E37 26 FA               BNE    GROU1
```

```
00470 3E39 E6 01          LDA B  1,X
00480 3E3B 31       GR0U2 INS
00490 3E3C 34             DES
00500 3E3D 96 18          LDA A  AT0D
00510 3E3F 36             PSH A
00520 3E40 5A             DEC B
00530 3E41 27 04          BEQ    0N
00540 3E43 02             N0P
00550 3E44 7E 3E3B        JMP    GR0U2
00560 3E47 08       0N    INX
00570 3E48 08             INX
00580 3E49 E6 00          LDA B  X
00590 3E4B 27 4E    GR0PK BEQ    INVLD
00610 3E4D A6 01          LDA A  1,X
00630 3E4F 27 05    L0PIN BEQ    GETDA
00640 3E51 95 1A          BIT A  PIRB
00650 3E53 4A             DEC A
00660 3E54 20 F9          BRA    L0PIN
00670 3E56 96 18    GETDA LDA A  AT0D
00680 3E58 36             PSH A
00690 3E59 5A             DEC B
00700 3E5A 27 EB          BEQ    0N
00710 3E5C 34             DES
00720 3E5D 31             INS
00725 3E5E 02             N0P
00730 3E5F 7E 3E4B        JMP    GR0PK
01070 3E62 8E 1018 0UTD   LDS    #SSTAC
01080 3E65 8D 3A          BSR    L00KFL
01095 3E67 44             LSR A
01100 3E68 B1 3FAE        CMP A  CANADD
01110 3E6B 26 2E          BNE    INVLD
01120 3E6D 8D 47          BSR    SEREA8
01130 3E6F B7 1009        STA A  H0USE1
01200 3E72 8D 2D          BSR    L00KFL
01210 3E74 43             C0M A
01220 3E75 44             LSR A
01230 3E76 B1 3FAE        CMP A  CANADD
01240 3E79 26 20          BNE    INVLD
01330               * GR0UP
01370 3E7B 8D 24          BSR    L00KFL
01380 3E7D 84 FE          AND A  #$F
01385 3E7F B7 1005        STA A  GR0UP
01550               * # 0F GR0UP
01560 3E82 8D 1D          BSR    L00KFL
01570 3E84 44             LSR A
01580 3E85 B7 1006        STA A  N0BLKS
01590 3E88 8D 17          BSR    L00KFL
01600 3E8A 84 FE          AND A  #$F
01610 3E8C 26 02          BNE    *+4
01620 3E8E 86 01          LDA A  #$0
01690 3E90 B7 1007        STA A  RATE
01692 3E93 8D 21          BSR    SEREA8
```

```
01694 3E95 B7 1008          STA A  HOUSE2
01700 3E98 7E 3F59          JMP    TURNON
03900                  * SUBROUTINES
04050                  *TERMINATION ROUTINES
04060 3E9B C6 0A    INVLD  LDA B  #$0A
04070 3E9D D7 1A           STA B  PIRB
04080 3E9F 20 FA           BRA    INVLD
05002 3EA1 86 0C    L00KFL LDA A  #$0C
05004 3EA3 97 1A           STA A  PIRB
05005 3EA5 86 18           LDA A  #$18
05010 3EA7 BD 3F3B  WAITR  JSR    DS
05015 3EAA 4A              DEC A
05020 3EAB 27 EE           BEQ    INVLD
05030 3EAD D6 1A           LDA B  PIRB
05040 3EAF C5 01           BIT B  #$01
05050 3EB1 27 F4           BEQ    WAITR
05100 3EB3 BD 3F3B         JSR    DS
05220 3EB6 7F 1001  SEREA8 CLR    M2
05230 3EB9 86 08           LDA A  #$08
05231 3EBB B7 1002         STA A  COUNT
05255 3EBE 86 04    SERL0P LDA A  #04
05260  EC0 97 1A           STA A  PIRB
05263 3EC2 8D 16           BSR    MS
05300 3EC4 96 1A           LDA A  PIRB
05310 3EC6 84 01           AND A  #$0
05350 3EC8 BB 1001         ADD A  M2
05353 3ECB C6 06           LDA B  #$06
05356 3ECD D7 1A           STA B  PIRB
05360 3ECF 7A 1002         DEC    COUNT
05370 3ED2 27 06           BEQ    MS
05380 3ED4 48              ASL A
05385 3ED5 B7 1001         STA A  M2
05390 3ED8 20 E4           BRA    SERL0P
05450 3EDA 39       MS     RTS                MS
05501 3EDB 16       PARITY TAB
05502 3EDC F8 1000         EOR B  M
05503 3EDF F7 1000         STA B  M
05509 3EE2 39              RTS                PARITY
05512 3EE3 C6 07    PAT0SE LDA B  #07
05514 3EE5 F7 1002         STA B  COUNT
05516 3EE8 7F 1000         CLR    M
05520 3EEB B7 1001  PT0S   STA A  M2
05530 3EEE 84 80           AND A  #$8
05540 3EF0 8D 2B           BSR    CHIP
05582 3EF2 8D E7           BSR    PARITY
05595 3EF4 B6 1001         LDA A  M2
05600 3EF7 48              ASL A
05610 3EF8 7A 1002         DEC    COUNT
05620 3EFB 26 EE           BNE    PT0S
05622 3EFD 8D DC           BSR    PARITY
05624 3EFF 4D              TST A
05626 3F00 27 04           BEQ    Z01
```

```
05628 3F02 8D 06          BSR     ONE1
05630 3F04 20 1D          BRA     CHIP1
05634 3F06 C6 08    Z01   LDA B   #ZER
05636 3F08 8D 35          BSR     BTRATE
05642 3F0A 8D AA    ONE1  BSR     SEREA8
05644 3F0C 8D A8          BSR     SEREA8
05645 3F0E C6 01          LDA B   #$0
05646 3F10 F7 1004        STA B   XRATE+1
05648 3F13 F6 1007        LDA B   RATE
05650 3F16 F7 1003        STA B   XRATE
05652 3F19 20 31          BRA     ØPS
05660 3F1B 20 C6    PASTEP BRA    PATØSE
05700 3F1D 27 08    CHIP  BEQ     Z0
05710 3F1F C6 00          LDA B   #ØN
05725 3F21 8D 1C          BSR     BTRATE
05730 3F23 C6 08    CHIP1 LDA B   #ZER
05740 3F25 20 06          BRA     MEET
05750 3F27 C6 08    Z0    LDA B   #ZER
05765 3F29 8D 14          BSR     BTRATE
05770 3F2B C6 00          LDA B   #ØN
05780 3F2D 20 10    MEET  BRA     BTRATE
05800 3F2F A6 00    BITS9 LDA A   X
05810 3F31 8D B0          BSR     PATØSE
05815 3F33 09             DEX
05820 3F34 86 80          LDA A   #$8
05825 3F36 B4 1000        AND A   M
05830 3F39 20 E2          BRA     CHIP
05880 3F3B C6 20    DS    LDA B   #$20
05890 3F3D 20 05          BRA     DSJMP
05900 3F3F D7 1A    BTRATE STA B  PIRB
05905 3F41 F6 1007        LDA B   RATE
05910 3F44 F7 1003  DSJMP STA B   XRATE
05920 3F47 C6 2D    SET2  LDA B   #$2D
05925 3F49 F7 1004        STA B   XRATE+1
05930 3F4C 8D 8C    ØPS   BSR     MS
05940 3F4E 7A 1004        DEC     XRATE+1
05950 3F51 26 F9          BNE     ØPS
05960 3F53 7A 1003        DEC     XRATE
05970 3F56 26 EF          BNE     SET2
05980 3F58 39             RTS                    DS,BTRATE
06500               * XMTR TURN ØN
06550 3F59 86 0E    TURNØN LDA A  #$0E
06560 3F5B 97 1A          STA A   PIRB
06600 3F5D 4F             CLR A
06610 3F5E 43             CØM A
06620 3F5F 8D BA          BSR     PASTEP
06623 3F61 4F             CLR A
06624 3F62 43             CØM A
06625 3F63 8D B6          BSR     PASTEP
06630 3F65 86 F0          LDA A   #$F
06640 3F67 8D B2          BSR     PASTEP
06641 3F69 86 0C          LDA A   #$0
```

```
06642 3F6B 97 1A          STA A  PIRB
06643 3F6D BD 3EDA        JSR    MS
06650 3F70 86 A6          LDA A  #$A
06660 3F72 8D A7          BSR    PASTEP
06667 3F74 8D BB          BSR    BITS9+2
06670 3F76 B6 1008        LDA A  HOUSE2
06675 3F79 8D B6          BSR    BITS9+2
06680 3F7B B6 1009        LDA A  HOUSE1
06690 3F7E 8D B1          BSR    BITS9+2
06700 3F80 B6 1005        LDA A  GROUP
06710 3F83 5F             CLR B
06720 3F84 48             ASL A
06730 3F85 59             ROL B
06740 3F86 48             ASL A
06750 3F87 59             ROL B
06770 3F88 C0 13          SUB B  #$1
06780 3F8A 43             COM A
06790 3F8B 50             NEG B
06830 3F8C F7 1000        STA B  M
06840 3F8F B7 1001        STA A  M+1
06850 3F92 FE 1000        LDX    M
06875 3F95 7D 1006        TST    NOBLKS
06880 3F98 26 03    GRP   BNE    *+5
06882 3F9A 7E 3E9B        JMP    INVLD
06885 3F9D 86 08          LDA A  #$0
06886 3F9F B7 1005        STA A  GROUP     EQUIV. COUNTG
06890 3FA2 8D 8B    OPG   BSR    BITS9
06895 3FA4 7A 1005        DEC    GROUP
06896 3FA7 26 F9          BNE    OPG
06900 3FA9 7A 1006        DEC    NOBLKS
06910 3FAC 20 EA          BRA    GRP
06915 3FAE 00       CANADD FCB    CANCHA
06950 3FAF 0000           FDB    TIMOUT
06960 3FB1 00       TABL  FCB    00
07900 3FFE                ORG    $3FFE
07910 3FFE 3E00           FDB    $3E00
08000                   * SCRATCH & DATA MEMOR
08001 1000                ORG    $1000
08005 1000 00       M     FCB    00
08010 1001 00       M2    FCB    00
08015 1002 00       COUNT FCB    00
08020 1003 CC       XRATE FCB    $CC
08030 1004 CC             FCB    $CC
08040 1005 00       GROUP FCB    $00
08045 1006 00       NOBLKS FCB   $00
08050 1007 00       RATE  FCB    $00
08051 1008 00       HOUSE2 FCB   00
08052 1009 00       HOUSE1 FCB   00
08055 1018                ORG    $1018
08060 1018 00       SSTACK FCB   00
09000                     END
```

SYMBOL TABLE

TIMOUT	0000	ATOD	0018	DDRA	0018	CRA	0019	CRB	001B
DDRB	001A	PIRB	001A	XON	000E	XOFF	0002	PWROFF	000A
CANCHA	0000	ONE	0000	ZERO	0008	POWER	3E0F	AQUIRE	3E13
ED	3E22	WAITO	3E26	PANIC	3E2C	GROU1	3E33	GROU2	3E3B
ON	3E47	GROPK	3E4B	LOPIN	3E4F	GETDA	3E56	OUTD	3E62
INVLD	3E9B	LOOKFL	3EA1	WAITR	3EA7	SEREA8	3EB6	SERLOP	3EBE
MS	3EDA	PARITY	3EDB	PATOSE	3EE3	PTOS	3EEB	Z01	3F06
ONE1	3F0A	PASTEP	3F1B	CHIP	3F1D	CHIP1	3F23	ZO	3F27
MEET	3F2D	BITS9	3F2F	DS	3F3B	BTRATE	3F3F	DSJMP	3F44
SET2	3F47	OPS	3F4C	TURNON	3F59	GRP	3F98	OPG	3FA2
CANADD	3FAE	TABL	3FB1	M	1000	M2	1001	COUNT	1002
XRATE	1003	GROUP	1005	NOBLKS	1006	RATE	1007	HOUSE2	1008
HOUSE1	1009	SSTACK	1018						

RUN COMPLETE.

APPENDIX B

Underground Telemetry Data Acquisition

Memo from Dr. Shunk

November 6, 1974

MEMO TO DISTRIBUTION

Subject: Underground Telemetry Data Acquisition

Author: Dr. R. A. Shunk

The programmable data acquisition rate for the ytterbium gages being proposed for Husky Pup needs to be defined in more detail so Develco can set up their electronics. As an aid to establishing these numbers, the ytterbium data from Dido Queen,* 150 foot, and Husky Ace,* 180 foot, were run through a digital data acquisition simulation. Only the 150 foot gage was digitized at a variable rate. The data were artificially terminated to zero which is necessary for the filter analysis. A 10 kHz second order filter was applied to the signal with damping factors of from .8 to 1.5. The underdamped filter does not look good and will also ring on transient noise. A damping factor of between 1 and 2 is recommended.

The only channel that appears to be critical in terms of programming the data acquisition rate seems to be the 5 kb one. Here, the digitizing was started about 0.5 msec. before the signal (a purely arbitrary time) and run at 24 μsec./point for 1.2 msec. (another arbitrary time) to see if this digitizing rate was adequate for defining the signal rise and peaks. The digitizing rate was switched to 100 μsec./point for the remainder of the signal.

Figure 1 shows the raw signal from Dido Queen as reproduced from the data. 125 points were necessary. Figure 2 shows the raw signal from Dido Queen, 150 foot, digitized as discussed. A spline fit was used to derive the curve from the original data. When the signal was passed through a 10 kHz filter with a damping factor of 1.5 and digitized as discussed, the record in Figure 3

*Ytterbium Gage Measurements in Dido Queen and Husky Ace, Final Report, Nov. 1973. C. W. Smith, SRI.

is obtained. The narrow spikes are pretty well washed out by the filter but the signal is quite well resolved otherwise. Figure 4 shows the effect of the filter on the rise. It would appear that the initial digitizing rate could be dropped to 48 μsec./point and still recover the signal with good resolution. Incidentally, the signal has not been digitized with 8 bit resolution for say, twice the signal amplitude equal to full scale. The sampling time has also been assumed to be very short with respect to the sample length. If necessary, both of these assumptions can be changed.

Figure 5 shows the result of halving the initial digitizing rate while keeping the other parameters the same. A little more detail is lost but the loss is not as pronounced as that caused by the 10 kHz filter. 99 points were necessary.

The Husky Ace 180' (2.6 kb) data was treated similarly except the digitizing rate was held at 0.1 msec./point. Digitizing was started 1. msec ahead of the data as shown in Figure 6. On a test this could be 1 to 2 msec., depending on the estimated variation of the material wave speed at kb loadings. This will increase the number of stored points by 15 to 20. The digitizing rate was changed to 0.2 msec/point to see how the data would look. This is shown in Figure 7. In the 0.1 msec./point, 372 pts were necessary for the assumed 37.2 msec of recording time. At a rate of 0.2 msec./point, 186 points were necessary. Comparisons of Figures 7 and 8 show no discernable difference in the spline fitted data. The 10 kHz filter has no observable effect on this data as a bandwidth of about 7 kHz is all that is necessary for this signal.

It appears that the digitizing on this last channel could be started at shortly before zero time and be allowed to run until core is filled, an elapsed time of about 0.05 sec.

The number of storage points that actually contain useful data in both cases is much less than the available storage. It appears that time multiplexing of data in these kinds of experiments could be advantageous and could make the system much more valuable. That is, either simultaneous multiplexing of two channels whose signals are coming in at about the same time or sequential recording of signals spaced in time, is possible. This is a more complex operating mode than single channel recording but may make the system more cost effective for use on underground tests.

RAS:md

DISTRIBUTION
Maj. B. H. Ellis, DNA/FC
Dr. B. A. Hartenbaum, RDA
Mr. N. Gantick, DNA/FC

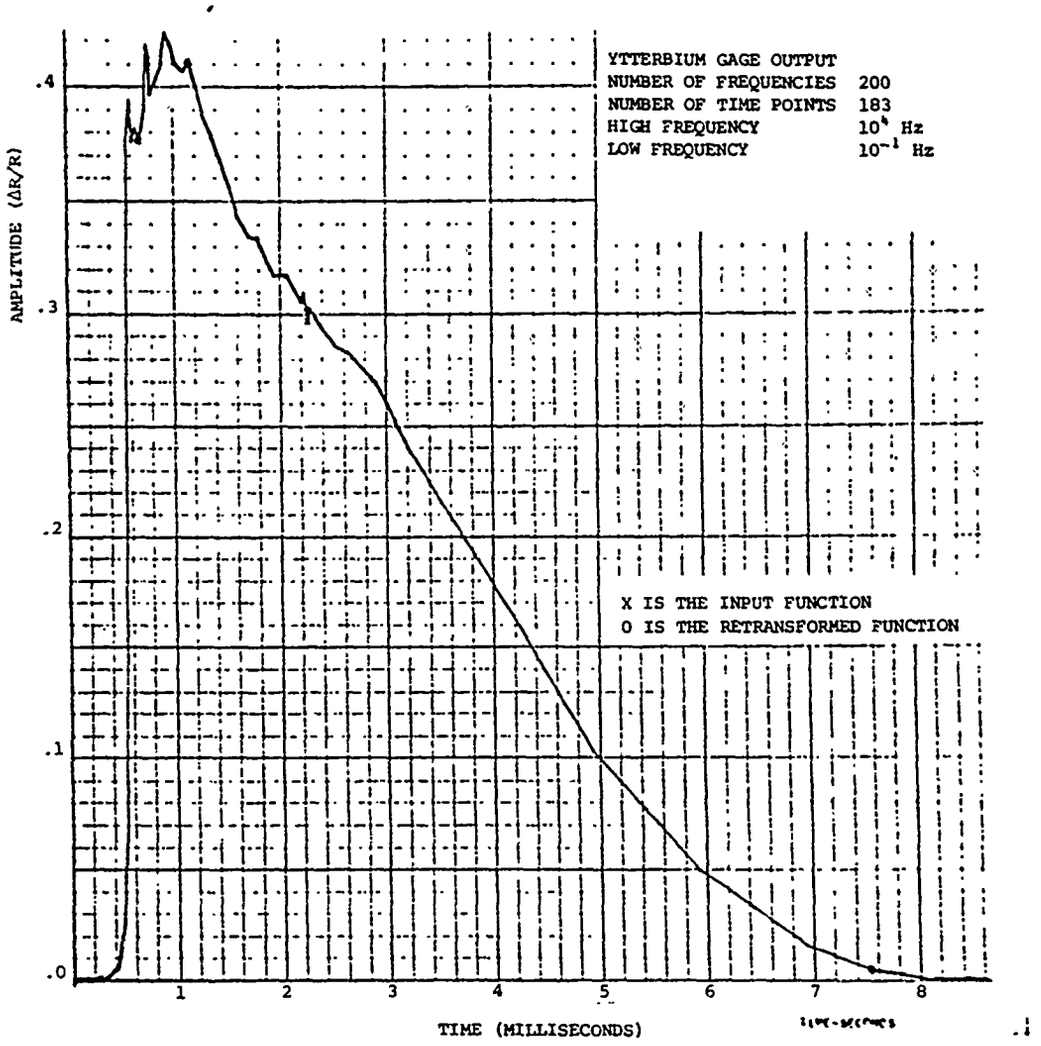


Fig. 1. The Ytterbium Gage Output ($\Delta R/R_o$) vs. Time on Dido Queen, 150 feet.

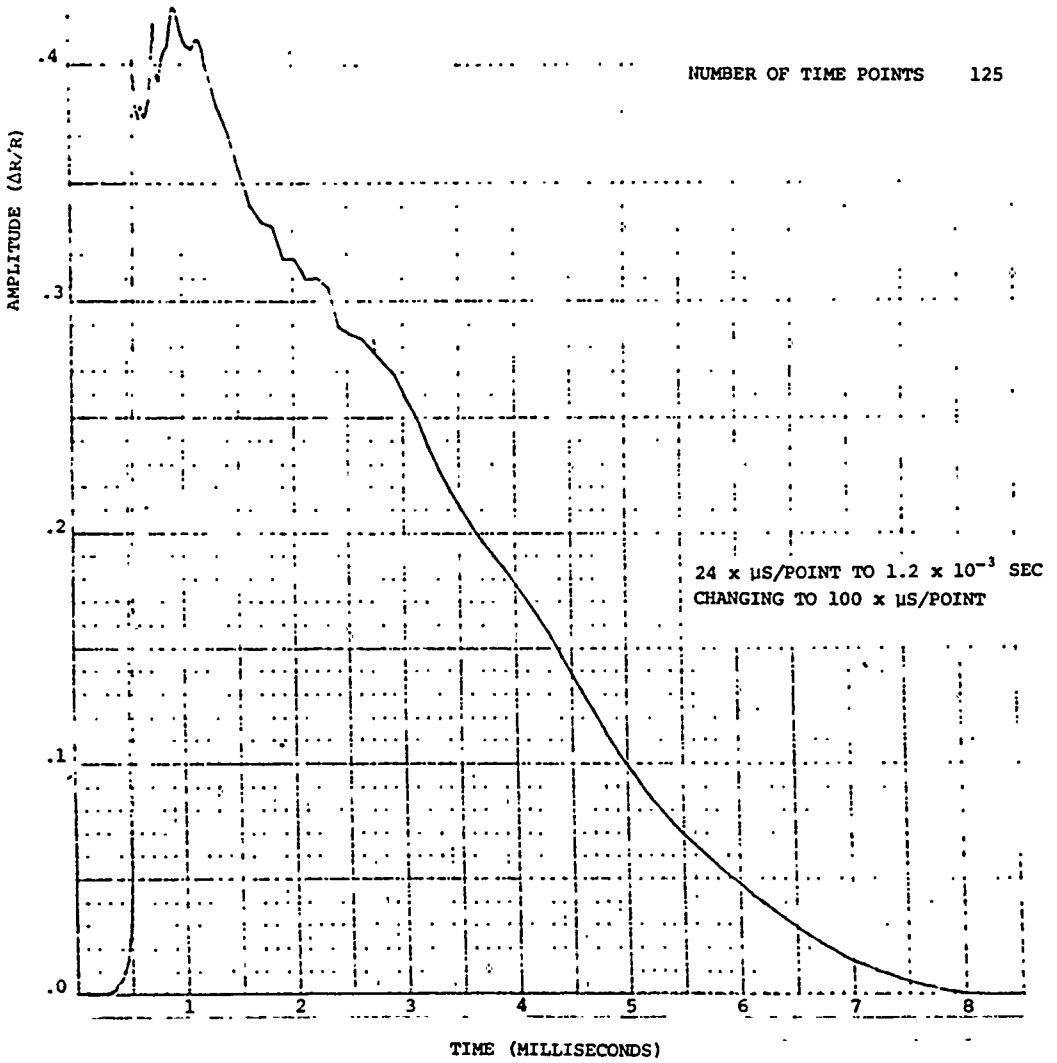


Fig. 2. The Ytterbium Gage Output ($\Delta R/R_o$) from Fig. 1 Digitized as Shown.

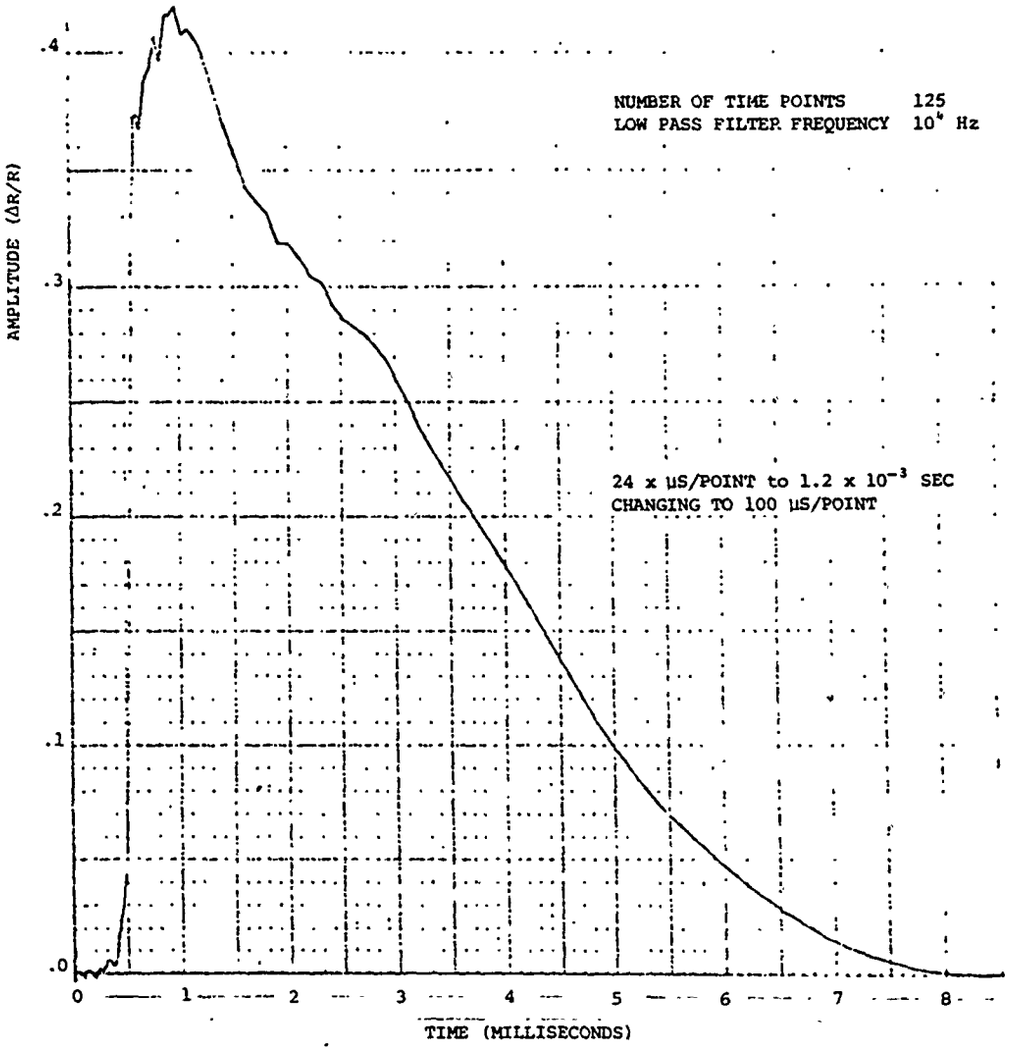


Fig. 3. The Ytterbium Gage Output from Fig. 1 ($\Delta R/R_o$) Filtered and Digitized.

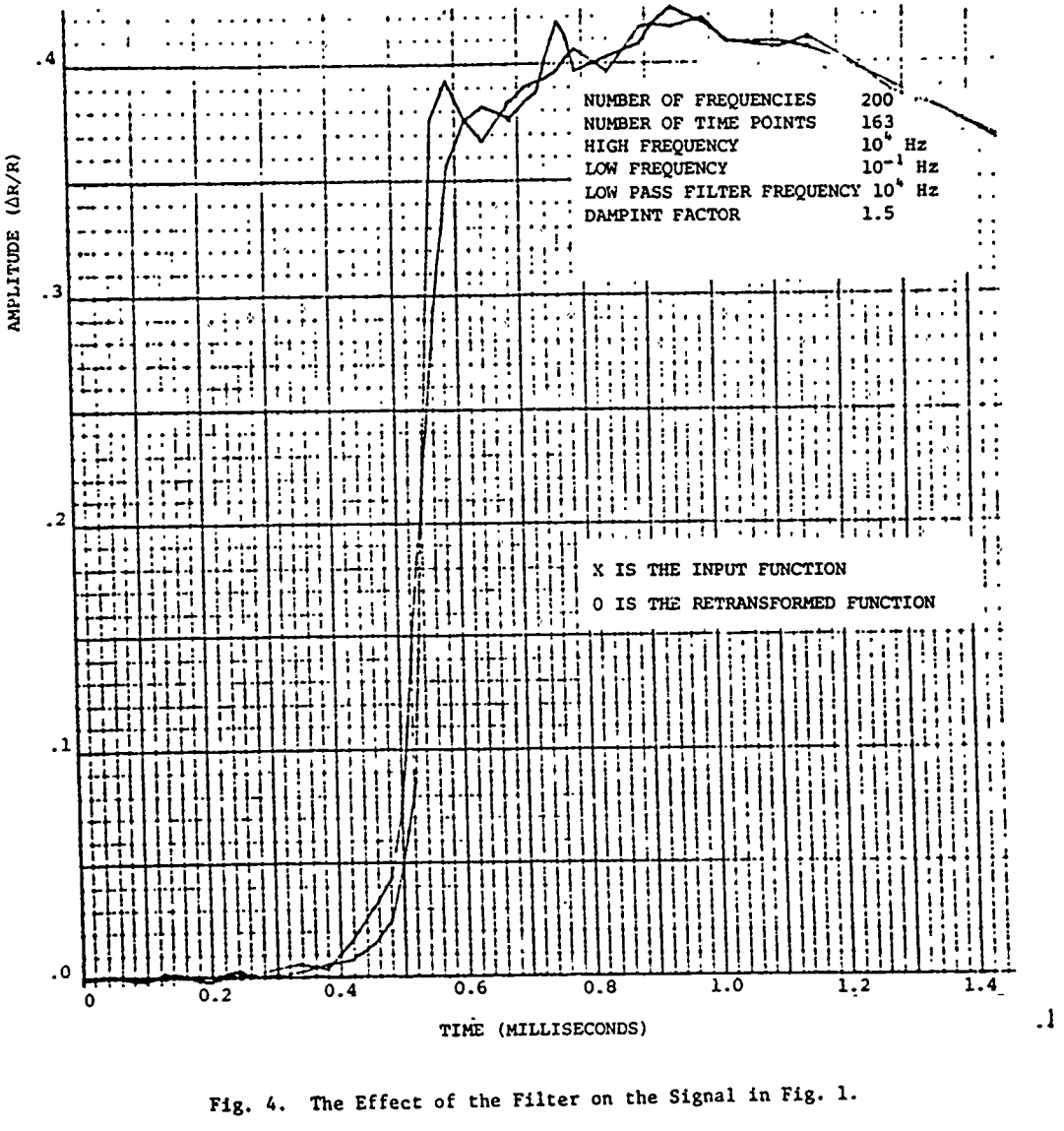


Fig. 4. The Effect of the Filter on the Signal in Fig. 1.

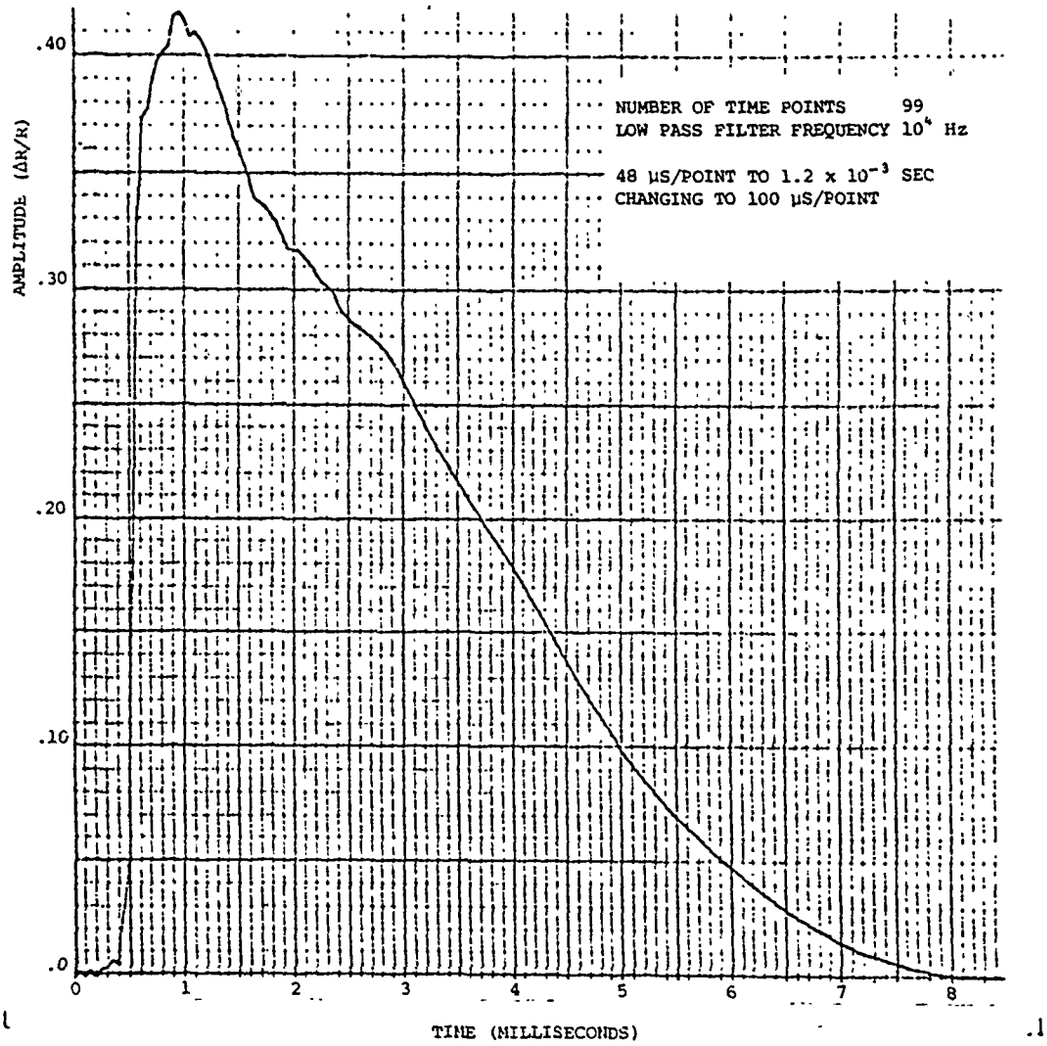


Fig. 5. The Ytterbium Gage Output ($\Delta R/R_o$) from Fig. 1 Filtered and Digitized at One-Half the Rate as in Fig. 3.

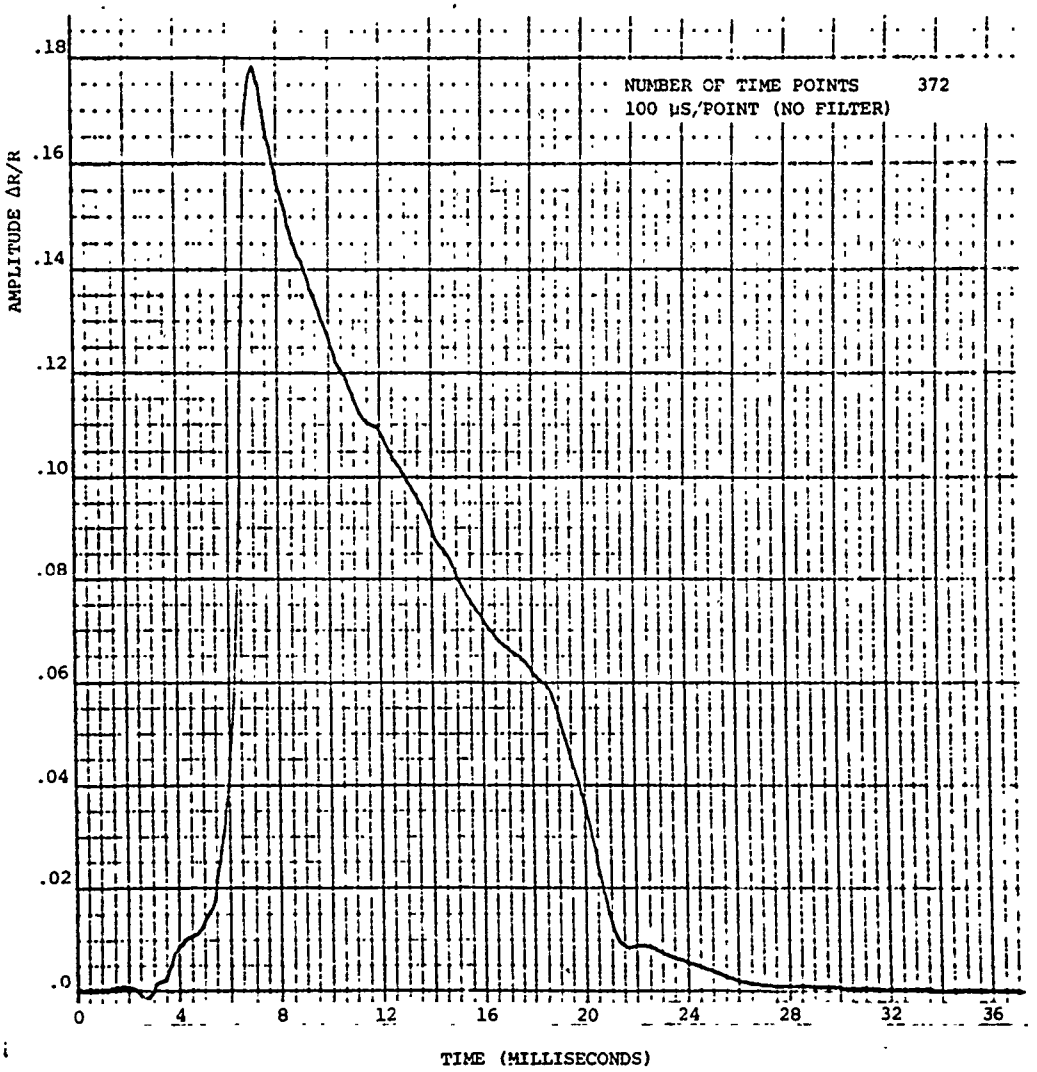


Fig. 6. The Ytterbium Gage Output ($\Delta R/R_o$ from Husky Ace, 180 Feet Digitized as Shown.

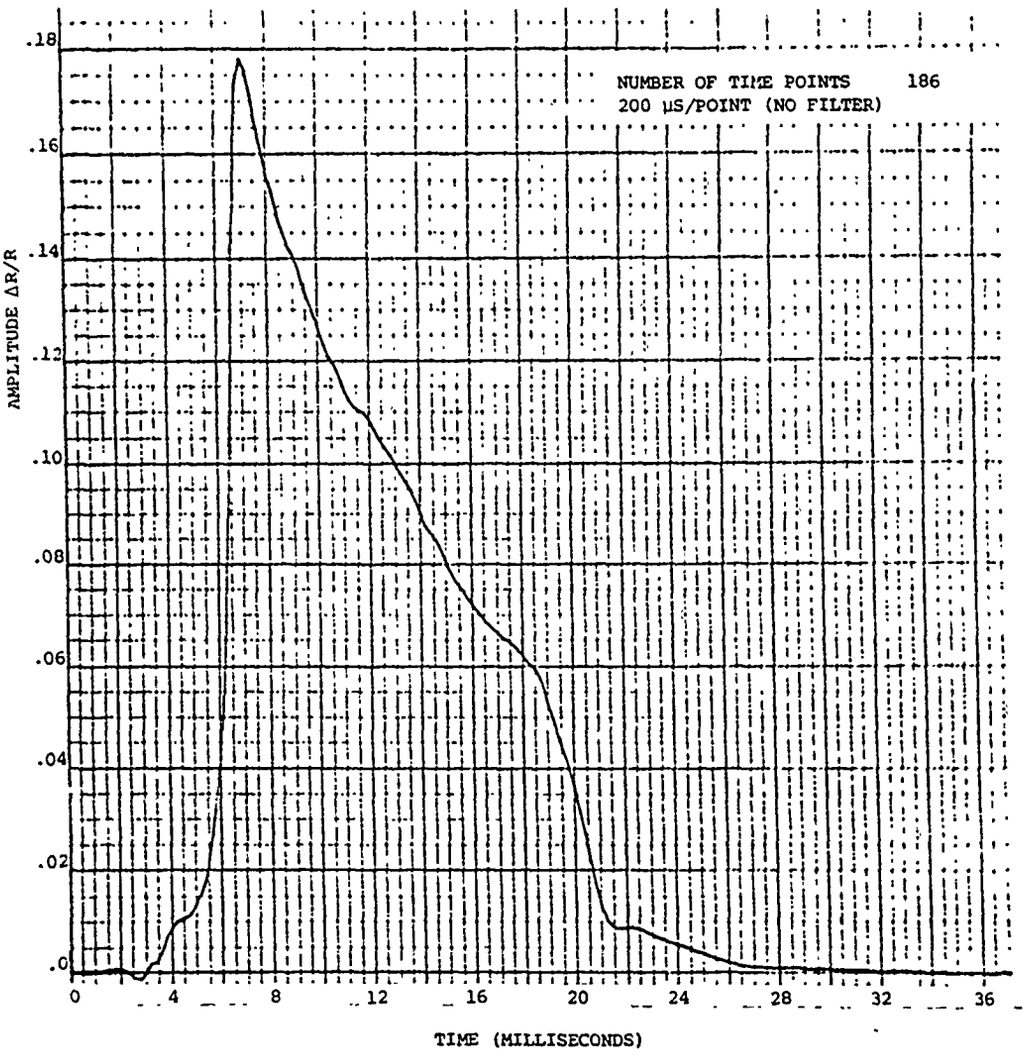


Fig. 7. The Ytterbium Gage Output ($\Delta R/R_o$) from Husky Ace, 180 Feet, Digitized at One-Half the Rate as in Fig. 6.

APPENDIX C
UNDERGROUND EMP CALCULATIONS
Memo from Dr. vanLint

R & D ASSOCIATES
Post Office Box 3580
Santa Monica,
California, 90403

V. van Lint, Consultant*

February 25, 1975

Commander
Field Command
Defense Nuclear Agency
Attn: Maj. H. Ellis
Kirtland Air Force Base, N. M. 87115

Dear Herb:

Enclosed is the report by Hrair Cabayan on the underground EMP calculations.

The model of the source is a cylindrical region of 1m radius and 2m length in which the axial electric field is approximately equal to the limiting value in the ground (2×10^6 V/m). I think this is a reasonable worst case source for a stemmed burst. In practice the source volume could be somewhat larger due to open spaces in the zero room, but there would also be some cancellation due to the radial distribution of emitted gammas. To a reasonable approximation one can scale linearly the effects of any other distribution of electric fields (with the same pulse shape) by calculating $\int \vec{E} d$ Vol over any reasonably small source region, (dimensions small compared to the 10m spacing to the cable) and rationing to the value 1.2×10^7 volts m^2 used in this calculation.

As you can see this model produces currents in points cables, at points at least 10m away from, the working point, either below or to the side, of 1100A peak or less. The rise time is much longer than I expected, namely ~.5-1 μsec. The decay times in the calculation are artifically long, as Hrair points out in his conclusions, and will in practice be 10 μsec or less.

This calculation assumed loss less earth. I don't see any way of getting a sharper rise time. Therefore, it appears to me that designing the shielding and filtering for $dI/dt = 10^9$ A/sec induced as bulk cable current, with a late time current of 10^3A lasting for 10 μsec. should be safe, as long as the source is not more extensive than was assumed here.

*"This work was performed by the consultant for RDA under a Defense Nuclear Agency contract. It has not been reviewed by RDA, nor does it necessarily represent an RDA opinion. Until it is reviewed it presents only the opinion of the consultant."

It's unfortunate that we don't have some real measurements to support these calculations. As you know, most of the available data are taken at very long ranges and above ground.

More accurate (less conservative) calculations could be performed, especially including earth conductivity. At this time I don't believe they are needed, because the underground cannisters should be able to survive the postulated pulse without difficulty.

Please call on me for any further discussions.

Sincerely yours,

Victor A. J. van Lint

VAJvL:jt
Enclosure

cc: R. Schaeffer/RDA
W. Graham/RDA

UGT EMP CALCULATIONS

1. MODEL

For calculating the currents induced on a nearby cable due to an underground test, the following model has been used:

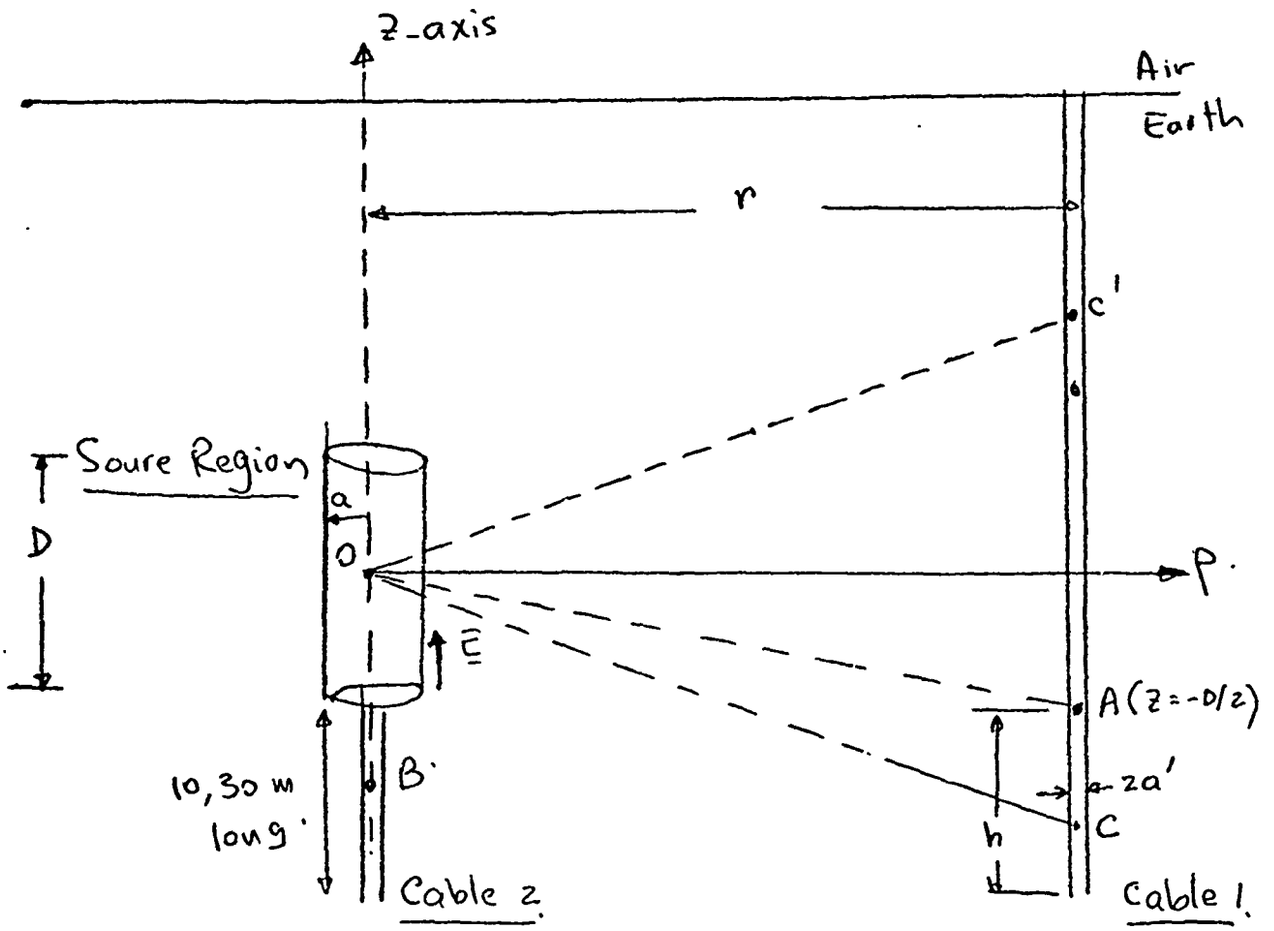


Figure 1. Sketch of source region and cable

The electric fields acting as sources are traveling on the surface of a cylinder of length D and radius a. The coordinate system is taken with the z-axis along the axis of this cylinder with the origin at the mid-point of the cylinder. The E-field source is traveling in the positive z-direction with velocity v ($v = 3 \times 10^8$ m/sec). A cable of radius a' is assumed parallel to the cylinder at a distance r. It is slightly longer by a length h as shown in the diagram. Both cylinder and cable are submerged in earth which is assumed lossless and of relative dielectric constant $\epsilon_r = 10$.

The source field E (Fig. 2) has the following waveshape:

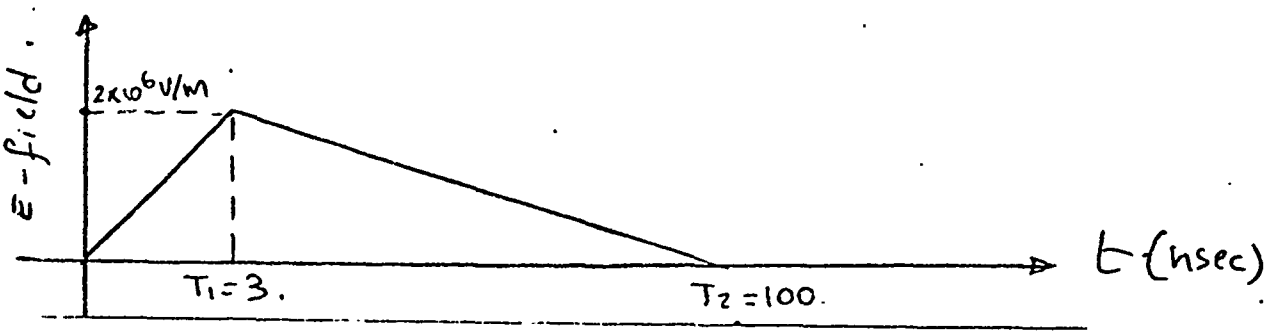


Figure 2. Time history of source

It has a rise time of 3 nsec, fall time of 100 nsec, and a peak of 2×10^6 V/m. The other parameters of the problem are

$a = 1$ m

$d = 2$ m

$r = 10$ m

$a' = 0.3$ cm

$h = 30$ m

The purpose of this exercise is to evaluate the currents i(t) induced in the cable at a point A as shown in Fig. 1.

2. ANALYSIS

2.1. Determination of the Irradiated E-Field

The irradiated E-fields from a source field E_0 on an infinity long cylinder of radius a are given by

$$E_z^- = E_0 \frac{1}{J_0(\bar{k}\, a)} J_0(\bar{k}\, \rho) \qquad (\rho < a)$$

(J_0 = zeroth order Bessel function of the first kind)

$$E_z^+ = E_0 \frac{1}{H_0^{(2)}(\bar{k}\, a)} H_0^{(2)}(\bar{k}\, \rho) \qquad (\rho \geq a),$$

($H_0^{(2)}$ = zeroth order Hankel function of the second kind)

where $\bar{k} = k\sqrt{\epsilon_r}$ ($k = \omega/c$: the wave vector in free space at frequency f). This assumes that the E-field has no variations in z. If now the E-field has a variation $e^{-jk_z z}$ with z, then

$$E_z^- = E_0\, e^{-jk_z z} \frac{1}{J_0(\bar{k}_\rho\, a)} J_0(k_\rho\, \rho) \qquad (\rho < a)$$

$$E_z^+ = E_0\, e^{-jk_z z} \frac{1}{H_0^{(2)}(\bar{k}_\rho\, a)} H_0^{(2)}(\bar{k}_\rho\, \rho) \qquad (\rho \geq a).$$

Here

$$\bar{k}_\rho = \sqrt{\bar{k}^2 - k_z^2}$$

If now the source field is made up of a continuous spectrum of frequencies

with the amplitude of each given by $E_z(k_z, \omega)$, then

$$E_z^- = \int_{-\infty}^{\infty} E_z(k_z, \omega)\, e^{-jk_z z}\, \frac{1}{J_0(\bar{k}_\rho a)}\, J_0(\bar{k}_\rho \rho)\, d k_z \qquad (\rho < a)$$

$$E_z^+ = \int_{-\infty}^{\infty} E_z(k_z, \omega)\, e^{-jk_z z}\, \frac{1}{H_0^{(2)}(\bar{k}_\rho a)}\, H_0^{(2)}(\bar{k}_\rho \rho)\, d k_z \qquad (\rho \geq a)$$

These equations can be used to calculate E-fields at all ρ if $E_z(k_z, \omega)$ is known at $\rho = a$. The wave shape f(t) shown in Fig. 2 has a Fourier transform

$$F(\omega) = E_0 \frac{1}{\omega^2} \frac{1}{T_1} \left[\frac{T_2}{T_2 - T_1}\, e^{-j\omega T_1} - \frac{T_1}{T_2 - T_1}\, e^{-j\omega T_2} - 1 \right], \quad (2.1.1)$$

for $\omega = 0$,

$$F(\omega) = \frac{1}{2} E_0 T_2 .$$

Since this wave is traveling at a velocity v,

$$\bar{F}(\omega) = \exp\left[-j \frac{\omega}{v}\left(z + \frac{D}{2}\right)\right] F(\omega) \qquad -\frac{D}{2} \leq z \leq \frac{D}{2} .$$

This wave exists only for $-D/2 \leq z \leq D/2$; it can be written as the Fourier transform of $E_z(k_z, \omega)$:

$$\bar{F}(\omega) = \int_{-\infty}^{\infty} E_z(k_z, \omega)\, e^{-jk_z z}\, d k_z$$

or

$$E_z(k_z, \omega) = \frac{1}{2\pi} \int_{-D/2}^{D/2} F(\omega) \exp\left[-jk\left(z + \frac{D}{2}\right)\right] e^{jk_z z}\, dz$$

$$= \frac{1}{\pi} F(\omega) \exp\left(-jk \frac{D}{2}\right) \frac{1}{k_z - k} \sin\left[(k_z - k)\frac{D}{2}\right].$$

[If $k = k_z$, $E_z(k_z, \omega) = (D/2\pi)\, F(\omega) \exp[-jk\,(D/2)]$.

Substituting the expressions for $E_z(k_z, \omega)$ into the integral expressions for E_z^- and E_z^+, we obtain

$$E_z^+(\omega) = \frac{2}{\pi} F(\omega) \int_{-\infty}^{\infty} e^{jx} \frac{\sin x}{x} \frac{H_0^{(2)}(\bar{k}_\rho \rho)}{H_0^{(2)}(\bar{k}_\rho a)} dx \qquad (\rho \geq a) \qquad (2.1.2)$$

$$E_z^-(\omega) = \frac{2}{\pi} F(\omega) \int_{-\infty}^{\infty} e^{jx} \frac{\sin x}{x} \frac{J_0(\bar{k}_\rho \rho)}{J_0(\bar{k}_\rho a)} \qquad (\rho < a) \qquad (2.1.2b)$$

where

$$x = (k_z - k)\frac{D}{2}$$

and

$$\bar{k}_\rho = \sqrt{\bar{k}^2 - k_z^2} \qquad (\bar{k} = k\sqrt{\epsilon_r})$$

$$\bar{k}_\rho^2 = \bar{k}^2 - k_z^2$$

$$= k^2(\epsilon_r - 1) - \frac{4x^2}{D^2} - \frac{4xk}{D} . \qquad (2.1.3)$$

Since an FFT will be taken, only positive frequencies ω will be needed. Therefore, k will always be positive. k_z varies from $-\infty$ to $+\infty$. If

$$k_z = \pm\bar{k}$$

or

$$x = \frac{kD}{2}\left[\pm\sqrt{\epsilon_r} - 1\right], \qquad (2.1.4)$$

then

$$\bar{k}_\rho = 0 .$$

- If

$$\bar{k}_\rho \to 0, \frac{H_0^{(2)}(\bar{k}_\rho \rho)}{H_0^{(2)}(\bar{k}_\rho a)} \to 1 ,$$

- if

$$\frac{kD}{2}\left[-\sqrt{\epsilon_r}-1\right] < x < \frac{kD}{2}\left[\sqrt{\epsilon_r}-1\right],$$

then

$$k_\rho^2 > 0 \quad \text{and} \quad \frac{H_0^{(2)}(\bar{k}_\rho \rho)}{H_0^{(2)}(\bar{k}_\rho a)}$$

has real arguments.

- If

$$x < \frac{kD}{2}\left[-\sqrt{\epsilon_r}-1\right]$$

or

$$x > \frac{kD}{2}\left[\sqrt{\epsilon_r}-1\right],$$

then

$$k_\rho^2 < 0 .$$

In this case,

$$\frac{H_0^{(2)}(\bar{k}_\rho \rho)}{H_0^{(2)}(\bar{k}_\rho a)} \rightarrow \frac{K_0(|\bar{k}_\rho| \rho)}{K_0(|\bar{k}_\rho| a)},$$

where K_0 is the modified Bessel function of the second kind which decays to zero as the argument increases to infinity.

Rewriting the expression for E_z^+,

$$E_z^+ = \frac{2}{\pi} F(\omega) \int_{-\infty}^{\infty} e^{jx} \frac{\sin x}{x} \frac{H_0^{(2)}(\bar{k}_\rho \rho)}{H_0^{(2)}(\bar{k}_\rho a)} dx .$$

The term

$$e^{jx}\,\frac{\sin x}{x} = \frac{1}{x}\left(\frac{1}{2}\sin 2x + j\sin^2 x\right)$$

can oscillate with a half-period of $\pi/2$ and decays away from zero as $1/x$. (It peaks at $x = 0$.)

The term

$$\frac{H_0^{(2)}(\bar{k}_\rho \rho)}{H_0^{(2)}(\bar{k}_\rho a)}$$

peaks when $x = kD/2\,[\pm\sqrt{\epsilon_r - 1}]$ which, for $\epsilon_r = 10$, peaks when $x \sim kD$ and $x \sim -2\,kD$. A sketch of these functions is shown in Figure 3. Here

$$\frac{\sin 2x}{2x}$$

is shown, together with

$$\frac{H_0^{(2)}(\bar{k}_\rho \rho)}{H_0^{(2)}(\bar{k}_\rho a)}.$$

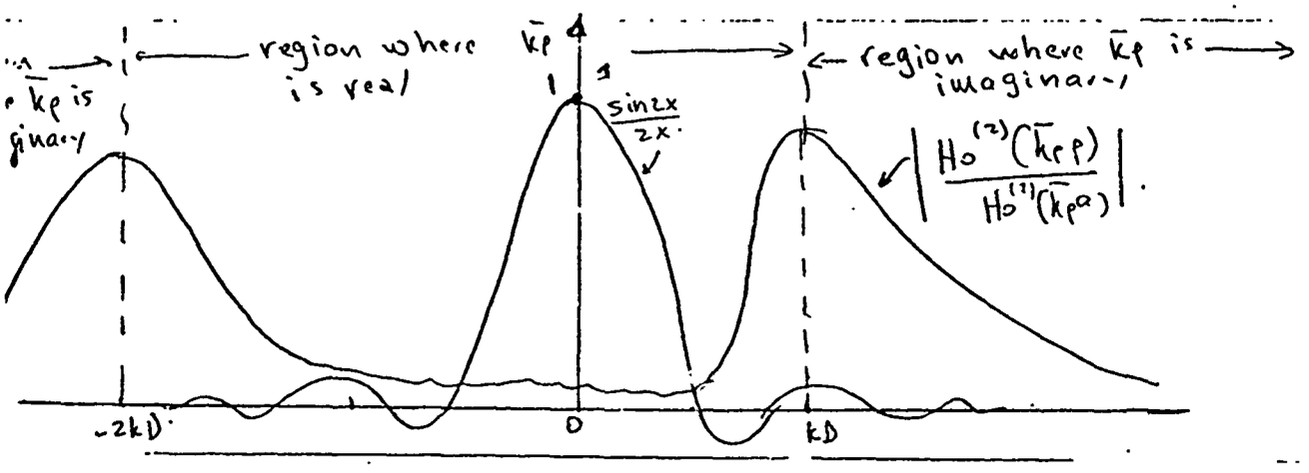


Figure 3. Sketch of integrand of E_z^+ integral

The product of these functions when integrated yields the field E_z at $\rho = r$ for a certain frequency ω. It is obvious that the integration need be done only for values of x around the origin.

As the frequency increases, k increases, and the region of interaction between the two curves decreases. This yields to heavy attenuation of the high-frequency components.

If the field is desired at a point such as B in Fig. 1, then the integral formulation for E_z^- with $\rho = 0$ should be used.

$$E_z^- = \frac{2}{\pi} F(\omega) \int_{-\infty}^{\infty} e^{jx} \frac{\sin x}{x} \frac{1}{J_0(\bar{k}_\rho a)} dx ,$$

If $\bar{k}_\rho \rightarrow 0$ $\qquad J_0(\bar{k}_\rho a) \rightarrow 1$,

if $\bar{k}_\rho \rightarrow$ real $\qquad J_0(\bar{k}_\rho a)$: no problem,

if $\bar{k}_\rho \rightarrow$ imaginary $\qquad J_0(\bar{k}_\rho a) \rightarrow I_0(|\bar{k}_\rho| a)$,

where I_0 is the modified Bessel function of the first kind.

2.2. Determination of Currents

The vertical field component E_z was determined in the previous section at point A (refer to Figure 1). For any point of coordinates z and ρ at which the fields are desired, the expressions are

$$E^{+}_{inc} = \frac{2}{\pi} F(\omega) \exp\left[-jk\left(\frac{D}{2} + z\right)\right] \int_{-\infty}^{\infty} \frac{\sin x}{x}$$

$$\times \frac{H_0^{(2)}(\bar{k}_\rho \rho)}{H_0^{(2)}(\bar{k}_\rho a)} \exp\left(-j2\frac{z}{D}x\right) dx \qquad (\rho \geq a) \qquad (2.2.1)$$

$$E^{-}_{inc} = \frac{2}{\pi} F(\omega) \exp\left[-jk\left(\frac{D}{2} + z\right)\right] \int_{-\infty}^{\infty} \frac{\sin x}{x}$$

$$\times \frac{J_0(\bar{k}_\rho \rho)}{J_0(\bar{k}_\rho a)} dx \qquad (\rho < a) \qquad (2.2.2)$$

Equations (2.2.1) and (2.2.2) represent the incident fields which impinge on the cables. The cables are assumed to be lossy with surface impedance Z_b given by

$$Z_b = \frac{\eta}{2\pi a'} \frac{I_0(\zeta a')}{I_1(\zeta a')} \qquad (2.2.3)$$

where

a' = radius of cable

$\eta = [j\omega\mu/\sigma]^{\frac{1}{2}}$

μ = permeability = $4 \times \pi \times 10^{-7}$

σ = conductivity [for copper cables, $\sigma = 5.8 \times 10^7$]

ω = angular frequency

I_0 = modified Bessel function of the first kind and zeroth order

I_1 = modified Bessel function of the first kind and first order

$\zeta = [j\omega\mu\sigma]^{\frac{1}{2}}$

The boundary conditions on the surface of the conductor are:

$$E_{inc} + E_s = Z_b I ; \quad H_{inc} + H_s = I/(2\pi a') \tag{2.2.4}$$

where

E_s: is the z component of the scattered E-field from conductor

H_{inc} and H_s: Incident and scattered Φ component of the H-fields

I: Current on the conductor

If Eqs. (2.2.4) are now specialized, the following expressions are obtained for the current (assuming the cable is infinity long).

For cable 1 as in Fig. 1,

$$I^+(k, z) = \omega\epsilon \frac{8}{\pi} F(\omega) \exp\left[-jk\left(\frac{D}{2} + z\right)\right] \int_{-\infty}^{\infty} \frac{\sin(x)}{x}$$

$$\times \exp\left(-j \frac{2z}{D} x\right) \frac{H_0^{(2)}(\bar{k}_\rho \rho)}{H_0^{(2)}(\bar{k}_\rho a)} \frac{dx}{\bar{k}_\rho^2 H_0^{(2)}(\bar{k}_\rho a') - j2\pi\omega\epsilon a' k_\rho Z_b H_1^{(2)}(\bar{k}_\rho a')} . \tag{2.2.5}$$

For cable 2,

$$I^-(k, z) = \omega\epsilon \frac{8}{\pi} F(\omega) \exp\left[-jk\left(\frac{D}{2} + z\right)\right] \int_{-\infty}^{\infty} \frac{\sin(x)}{x}$$

$$\times \exp\left(-j \frac{2z}{D} x\right) \frac{1}{J_0(\bar{k}_\rho a)} \frac{dx}{\bar{k}_\rho^2 H_0^{(2)}(\bar{k}_\rho a') - j2\pi\omega\epsilon a' \bar{k}_\rho Z_b H_1^{(2)}(\bar{k}_\rho a')} \tag{2.2.6}$$

where

ω Angular frequency

ϵ dielectric constant of earth

$F(\omega)$ defined in Eq. (2.1.1)

J_0 Bessel function of the first kind and zeroth order

k_ρ^2 defined in Eq. (2.1.3)

$H_0^{(2)}$ Hankel function of the second kind and zeroth order

$H_1^{(2)}$ Hankel function of the second kind and first order

Z_b surface impedance of wire

It is interesting to note several things. As pointed out in Section 2.1 for a given frequency k, k_ρ exhibits two zeros for values of x given in Eq. (2.1.4). If the surface impedance Z_b is set equal to zero, then the integrands in Eqs. (2.2.5) and (2.2.6) have singularities when $k_\rho^2 \to 0$, since the product $k_\rho^2 H_0^{(2)}(k_\rho a') \to 0$ as $k_\rho^2 \to 0$. Although the integral is bounded (the integrand is singular; however, the integral is finite if principal values are taken), a major problem is encountered in evaluating the integrals numerically. In fact, with $Z_b \neq 0$, as $k_\rho \to 0$, the integrands in Eqs. (2.2.5) and (2.2.6) become

$$\frac{\sin(x)}{x} \exp\left(-j \frac{2z}{D} x\right) \frac{1}{4\omega\epsilon Z_b} ,$$

and a singularity is thus avoided.

If k_ρ^2 is negative, and k_ρ is imaginary, then the integrand of Eq. (2.2.5) becomes

$$\frac{1}{x} \sin(x) \exp\left(-j \frac{2z}{D} x\right) \frac{K_0(|\bar{k}_\rho|\rho)}{K_0(|\bar{k}_\rho| a)} \frac{1}{\bar{k}_\rho^2 \frac{2j}{\pi} K_0(|\bar{k}_\rho| a') + 4\omega\epsilon a' Z_b |\bar{k}_\rho| K_1(|\bar{k}_\rho| a')} ,$$

and for Eq. (2.2.6),

$$\frac{1}{x} \sin(x) \exp\left(-j \frac{2z}{D} x\right) \frac{1}{I_0(|\bar{k}_\rho| a')} \frac{1}{\bar{k}_\rho^2 \frac{2j}{\pi} K_0(|\bar{k}_\rho| a') + 4\omega\epsilon a' Z_b |\bar{k}_\rho| K_1(|\bar{k}_\rho| a')}$$

where

K_0 modified Bessel function of the second kind and zeroth order,

K_1 modified Bessel function of the second kind and first order,

I_0 modified Bessel function of the first kind and zeroth order.

The integrals for the currents exhibit the same properties as those for the E-fields; namely, heavy attenuation at high frequencies and a need for the x-integral to be carried out only in a region close to the origin.

3. NUMERICAL RESULTS

A numerical program has been written to evaluate Eq. (2.2.5) and 2.2.6). From Eqs. (2.1.5) and (2.1.6), it is observed that for a given k, k_ρ^2 has two zeros as a function of x:

$$x_1 = \frac{-kD}{2}\left[\sqrt{\epsilon_r} + 1\right]$$

$$x_2 = \frac{kD}{2}\left[\sqrt{\epsilon_r} - 1\right].$$

The dependence of k_ρ^2 on x is sketched in Fig. 4.

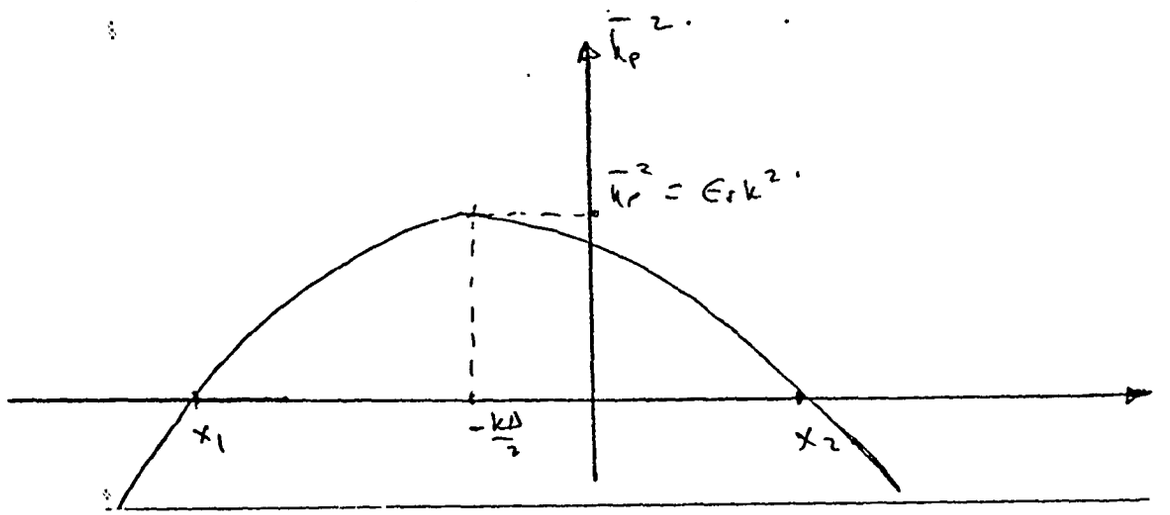


Figure 4. Sketch of $\bar{k}_\rho^2$ as a function of x

when $x_1 < x < x_2$, then k_ρ^2 is positive, and k_ρ is real. When $x < x_1$ or $x > x_2$, then k_ρ^2 is negative and k_ρ is purely imaginary. In performing the integrations in x, fine intervals were used for $x_1 < x < x_2$, and coarser intervals for $x < x_1$, and $x > x_2$. The integrations in x were carried from -20 π to +20 π, and that was found to be sufficient. For

small values of the argument k_ρ ($|k_\rho| < 10^{-6}$), the following approximate relations were used for the Bessel functions involved,

$$H_0^{(2)}(x) \cong 1 + j(0.074) - j\frac{2}{\pi}\log x$$

$$H_1^{(2)}(x) \cong j\frac{2}{\pi x}$$

$$K_0(x) \cong 0.116 - \log x$$

$$K_1(x) \cong \frac{1}{x}$$

$$J_0 \cong 1.$$

$$I_0 \cong 1.$$

Only for $|\overline{k}_\rho| > 10^{-6}$ were the special Bessel functions evaluated specifically.

The surface impedance Z_b given in Eq. (2.2.3) was evaluated by using the following relations for the functions I_0 and I_1

$$I_0(u\sqrt{j}) = \text{ber } u + j\,\text{bei } u$$

$$I_1(u\sqrt{j}) = \frac{\text{ber}_1 u + j\,\text{bei}_1 u}{j}$$

where ber_n and bei_n ($n = 0, 1$) are the Kelvin functions. Existing subroutines at IRT were used to evaluate these functions.

The current in cable 1 at location A is shown in Fig. 5 for D = 2 m. The peak current is 620 amps, and the rise time is ~0.5 to 1.0 μsec. The very long decay observed is due to the fact that the cable is assumed to be infinity long and because the earth has been assumed lossless. Once the current builds up in the cable, it has no way to dissipate itself except in the losses in the cable. For cable 2 at location B, the current response is shown in Fig. 6. The peak current is 1.1 kA, and the rise time is on the order of 1 μsec. Again, a slow decay time is observed.

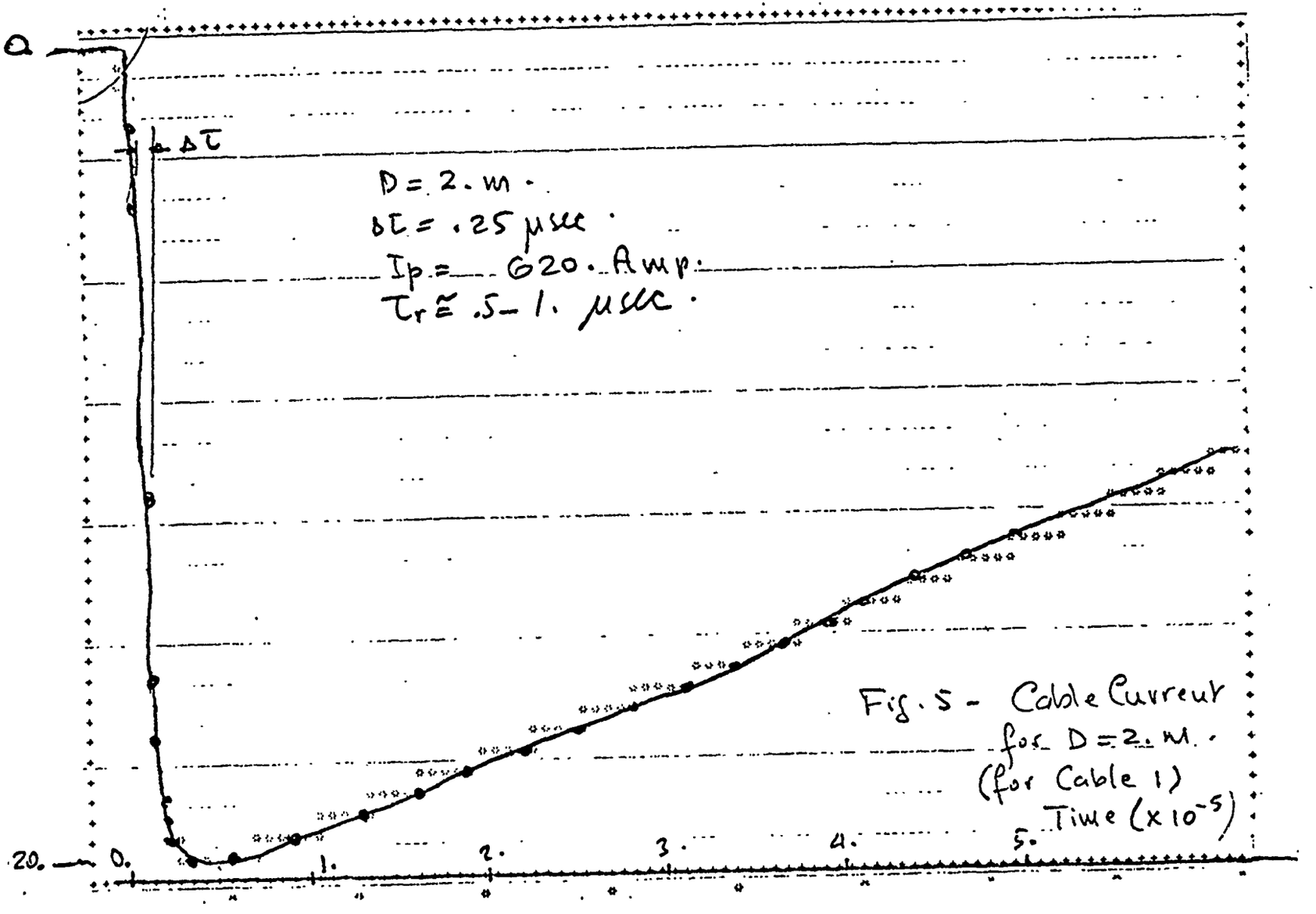


Fig. 5 - Cable Current for D = 2. M. (for Cable 1)

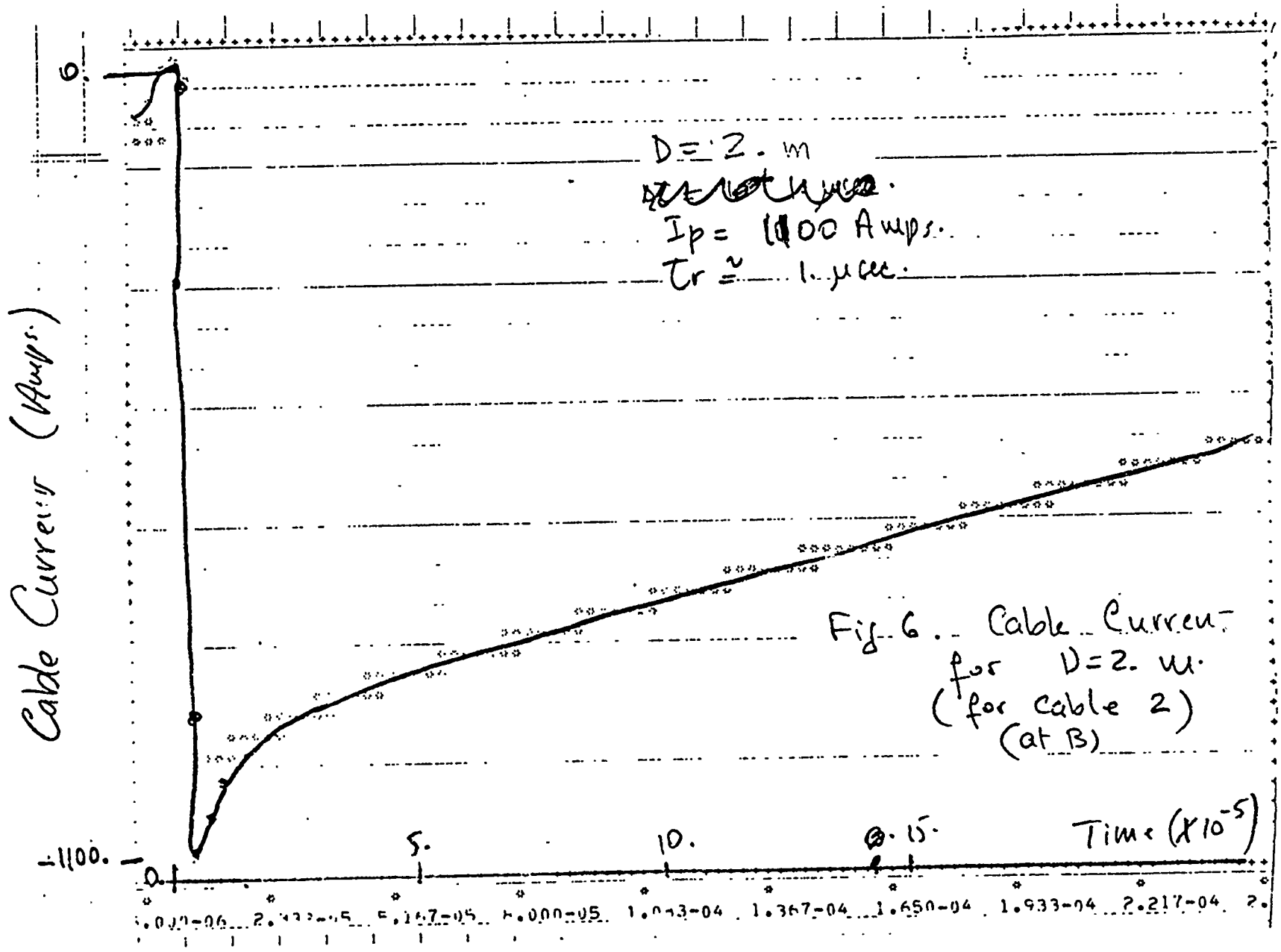


Fig. 6. Cable Current for D = 2. m. (for cable 2) (at B)

4. CONCLUSIONS

The results that have been obtained show long rise times and very long decay times. The very long decay time is mainly due to the assumption that the cable is infinity long. (This has been done in order to facilitate the computations; for finite length cables, the computation would have been considerably more costly.) In order to see why such long rise times and long decay times are experienced, refer to Fig. 1. The incident E-field from the source region reaches A in approximately 100 nsec (the distance from the source region to A is 10 m, and the dielectric constant of earth = 10) and lasts for about 100 nsec. For this 100-nsec period, the incident field builds up the currents at A. The fields reach points C and C' in Fig. 1 (positioned equidistant about the z = 0 axis) at a later time, since the distance OC is larger than OA, and induce currents at C and C' which now flow along the cable, and thus, the currents at A keep building up even though the fields at A have died down. Essentially, what happens is that current sources are generated along the line at successively delayed times. However, these current sources get weaker as the distance from the source to the point on the cable gets larger (the fields have to travel a longer distance). Since in the calculations the cable has been assumed infinity long, the results reflect the very long decay times observed in Figs. 5 and 6. However, the cable in question is only 1000 m long, and the farthest point on the cable from the source is approximately 1000 m. Since the velocity v of this field in earth is $v = c/\sqrt{\epsilon_r}$ (c is the speed of light, ϵ_r is the dielectric constant of earth), the cable will not see any incident fields at times larger than 10 μsec. Therefore, the response in Figs. 5 and 6 will quickly decay to zero after the first 10 μsec. Essentially therefore, the current responses have rise times on the order of 1 μsec and durations of 10 μsec.

This analysis neglects reflections that will occur at the ends of the finite length cable and will, in effect, increase the duration of the pulse.

But, if the assumption is made that the earth is lossy, the reflected current waves will be attenuated severely by the time they travel back. It is to be expected that the lossy earth will shorten both the rise time and the duration of the pulse.

APPENDIX D
EMP PROTECTION OF THE DEVELCO CANISTER
Memo from Dr. vanLint

Victor van Lint, Consultant* July 8, 1975

TO: Maj. H. Ellis

SUB: EMP Protection of the Develco Cannister

Bruce Hartenbaum and I visited Develco on July 1 to review the design of the EMP protection of their instrumentation cannister and the plans for testing the cannister.

The primary coupling of EMP energy to the instrument system will be by inducing currents in the long cables connecting the instrumentation cannister to the surface and to the sensors. Some fraction of these currents can appear on the signal wires, either through the transfer impedance of the long cable or by impedance introduced into the shield at its termination at the cannister. For this reason, it is desirable to protect the individual input leads going into the cannister so that large, high frequency spikes of energy are not allowed to propagate into the instrumentation lines. Since the cannister is not operating at the time the EM pulse hits, it is particularly important that this pulse not cause any permanent damage or change the logic of the data handling system.

As I understand it the timing and firing system is such that after the fidu signal is given to the cannister, which occurs some microseconds before the EMP arrives, subsequent signals on the control lines are unable to divert the logic from its preset sequence. This is a good philosophy and if it is correctly implemented will make the cannister immune to any EMP induced disturbances that don't actually produce permanent damage.

The protection of all the input leads has been achieved by bringing all the wires into a bulkhead, filtering them at the bulkhead with shunt capacitances of values between .01 and .3 microfarads, doing further signal conditioning where possible, and up to a second bulkhead at which the output lines are filtered with LC filters whose frequency response generally roles off in the vicinity of 10 kHz.

The filtering system uses standard commercial components. It is not the protection system that I would prefer. If the EM pulse had a fast rise time these components frequently have enough shunt inductance that very fast spikes could pass through. However, all of c calculations seem to indicate that the rise time of the EM pulse that can appear at the cannister is relatively slow (greater than 100 nanoseconds). Under these circumstances I can find no good argument for making any changes in this filtering system. It has the disadvantage

*"This work was performed by the consultant for RDA under a Defense Nuclear Agency contract. It has not been reviewed by RDA, nor does it necessarily represent an RDA opinion. Until it is reviewed it presents only the opinion of the consultant."

that dissipative elements (resistors) terms are not directly incorporated into the filters, therefore, the impedance of the shunt capacitance fighting against the source impedance which tends to be somewhat low (10's to 100's of ohms). Nevertheless, this system seems to be adequate for the current application and it would cause major difficulties to insert series resistances in line which are operating into 50 ohm loads.

Another protection factor which is desirable for severe EMP environments is to incorporate voltage limiting devices, such as surge arrestors. These can be in the form of non-linear breakdown devices or semiconductor diodes. I am convinced by Develco's argument that the risk in the current application of these devices failing in a short mode is enough to preclude using them. The argument is that the input circuits as designed can tolerate any spike up to the insulation breakdown voltage of the input cable. Therefore, further surge arresting would not have any useful effect. An additional difficulty is that in some of the instrument lines will be biased and therefore breakdown devices that depend upon the voltage returning to zero to recover cannot be used. I suspect that if I worked at it for awhile I would find I could conceive of an overvoltage protection scheme that I would like to see incorporated into this system, but again the argument that it is not needed in the present case is reasonably persuasive.

There are plans to test a section of input cable (about 30 feet long) together with the cable termination and the filtering bulkheads at PI by driving a current on the cable shield in a transmission line configuration. This seems like a reasonable test to me and the measurement of the signal that appears at the output of the second bulkhead should be a reasonable measure of the signal that might propagate through the filters in the underground test conditions. I believe it is important that both the down-hole cable and the SRI instrumentation cable be included in this test, and that the terminations of these cables at the cannister bulkheads be geometrically and physically the same as they will be made in the operational cannisters. The signals should be monitored with high enough frequency response to detect any high frequency spike that might propagate through the filtering network. If the signal is anywhere near the danger threshold for semiconductor devices then we should reconsider incorporating further protection, such as voltage limiting into the signal handling system. I also recommend that a test be performed in which one of the down-hole signal lines is driven hard enough to breakdown the filter capacitor on that line. An instrumentation is placed in the transducer lines to determine whether there is any significant cross-talk on the possible high frequency spikes produced by the capacitor breakdown into the signal handling chain. This experiment is desirable because it is possible that the long down hole cable will achieve high enough voltages to breakdown a capacitor. While this does not have any adverse affect on the circuits to which this cable is connected, because they have already performed their functions, if high frequency energy could do damage in the signal handling path this would be undersirable.

As planned, the direct drive test should be performed with about a 1 kiloamp with a rise time of 100 nanoseconds and a fall time of about 10 microseconds. It should be quite easy for PI to furnish a pulser that can perform such a task. It will be performed with a shorter length of down hole cable than is expected to be used in the real installation. As a first approximation the signal observed at the output of the filter should be acceptable even if it were multiplied by the ratio of the operational cable length to the test cable length. If the signal should not be acceptable under those circumstances, extra experiments may have to be performed to evaluate the scaling of the signal with cable length in particular to separate the contribution to the signal induced by the termination of the cable from that due to the cable transfer impedance. This term may be particularly important to the down-hole cable because I don't expect the transfer impedance of the foil-wrapped cable to be terrible good. Of course, this cable is also the one for which the test length will be only a small fraction of the operational length. If the transducer cable has a good solid sheath on it or a multible braid sheath, the transfer impedance of it should be quite good, and it is also not a terribly long cable in the operational situation

When the PI tests are performed I would like to have a look at the actual data that are generated to see if there are any surprises that require further attention. At that time, I can also advise whether there is enough safety margin that tests on the actual operational connisters will not be required. I recognize that it will be a pain in the nexk to do cable current drive tests on the cannisters with the long cables hooked up to them, and I hope it won't be necessary to perform these tests. However, should there be some significant uncertainties, particularly in regard to the scaling with cable length, a test out in the field with the cable connected up with the operational configuration of cable and cannister may be required.

Please call on me if I can be of any further assistance.

Sincerely yours,

Victor van Lint
Consultant

VVL:jt
cc: W. Graham
B. Hartenbaum

This report was taken from tape without Dr. van Lint's final approval.

APPENDIX E

EMP FILTER RESPONSE EFFECT ON MIGHTY EPIC DATA IN THE DEVELCO CANISTER

Memo from Dr. Shunk

MEMO TO DISTRIBUTION

FROM: R. A. Shunk/ T.A. Stough

SUBJECT: EMP Filter Response Effect on Mighty Epic Data in the Develco Canister

DATE: 29 June 1976

The preamplifier electronics used on Mighty Epic in the interface canisters that contained transducers recorded in the Develco system were designed with a 1000Ω output impedance. These preamplifiers were isolated from the Develco system by an EMP filter. The equivalent circuit is shown in Figure 1.

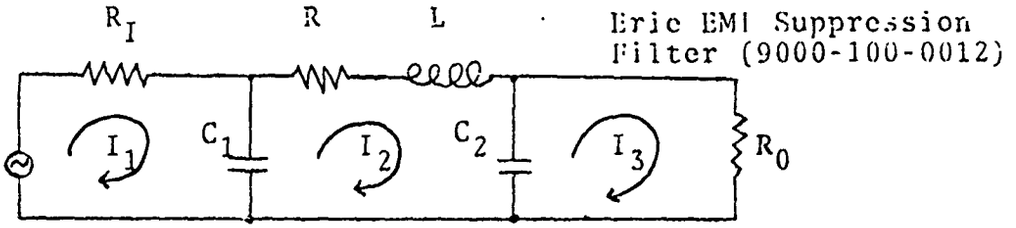


Figure 1. The Equivalent Circuit for the EMP Filter and Driving Electronics

A complete analysis of the filter was carried out using the electrical characteristics of the filter. The driving voltage used for the signal was the normalized signal from the ytterbium gage on Dido Queen at 180 feet range.* The signal was smoothly terminated to zero stress after the signal stopped. The fall time assumed was much longer than the rise time, so for the purpose of this analysis is not important.

The following equations represent this system:

$$R_I I_1 - \frac{j}{\omega C_1}(I_1 - I_2) = V \sin \omega t$$

* C. W. Smith, "Ytterbium Gage Measurements in Dido Queen and Husky Ace," SRI Final Report for Systems, Science and Software, Menlo Park, California (1973)

$$RI_2 + I_2 j\omega L - (I_2 - I_3)\frac{j}{\omega C_2} - (I_2 - I_1)\frac{j}{C_1\omega} = 0$$

and

$$R_0 I_3 - \frac{j}{\omega C_2}(I_3 - I_2) = 0$$

where $\omega = 2\pi f$

and R_I, R_0 are the input and output resistances respectively.

This system of equations was programmed for the Sandia Laboratory CDC 6600 computer in complex arithmetic. The SFFIT code, a Fourier transform and inversion code, was used to study the effect of the filter on the ytterbium gage data mentioned earlier and was plotted. The Fourier spectrum and phase of the driving voltage were modified by the filter and the resulting spectrum and phase inverted. The input and output signals are shown in Figure 2. Several different input resistances were tried. A 500Ω driving resistance produced a signal out of 88% of peak, a 100Ω driving resistor caused no appreciable deterioration of the signal. The rise time of the signal was increased from 1 msec to 5 msec to observe the effect of the filter and driving impedances on the output of the filter. The 1000Ω resistance is most important in the present application. In Figure 3 the change in peak and time lag of the peak are plotted vs. input rise time.

The 1 msec rise time (10 - 90%) signal shows a 22% peak decrease and the 5 msec rise time signal shows only a 6% decrease in peak value. There is a signal delay of about 2 msec, however. This delay was found to be insignificant for a 100Ω and lower input resistance.

Therefore, if signals with rise times of less than 3 milliseconds are encountered, reconstruction of the peak and initial portions of the wave may be advisable if an accurate time history is desired. Phase shift of the signal has also taken place so a change in the time base will also occur. The frequency band used on the signal was, incidentally, 0.01 to 1 kHz. It may be advisable to go to 2 kHz in an inversion scheme. This means that the signal to noise at 2 kHz should be small and that band limiting of the signal in the electronics and data reduction system be well above 2 kHz. The amplitude of the spectrum of this signal at 1 kHz is well over -20 db as shown in Figure 4. This spectrum shape is typical for signals of this type.

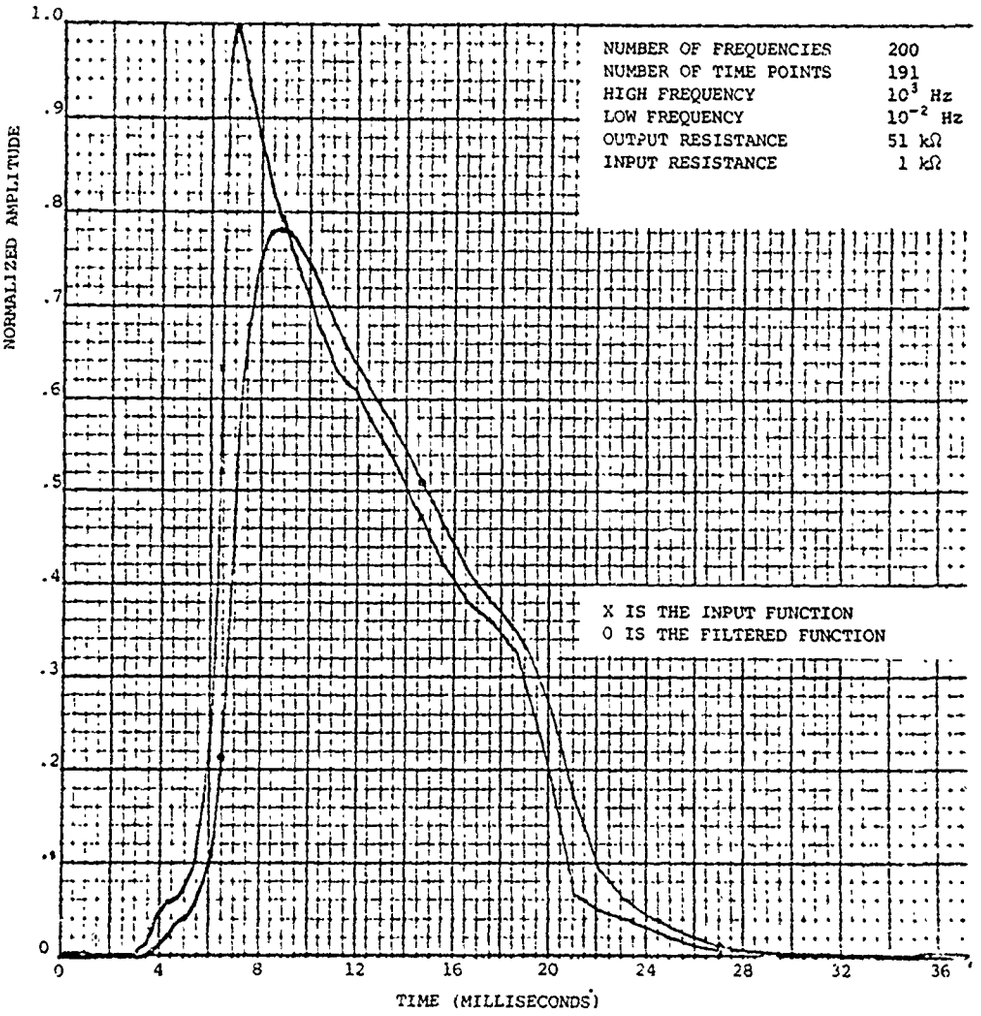


Figure 2 The Effect of the EMP Filter and a 1000 ohm Driving Impedance on an Ytterbium Gage Signal.

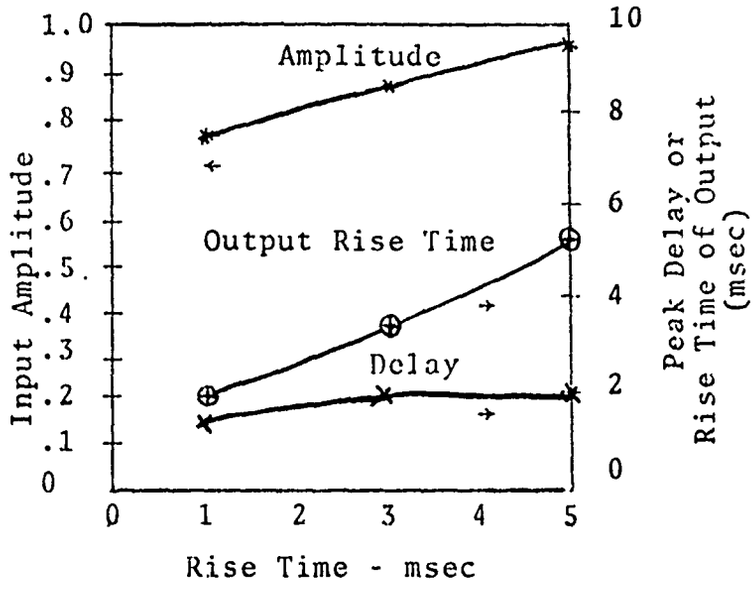


Figure 3. Rise Time vs. Normalized Output Amplitude and Peak Delay Time for a 1000Ω Input Resistance

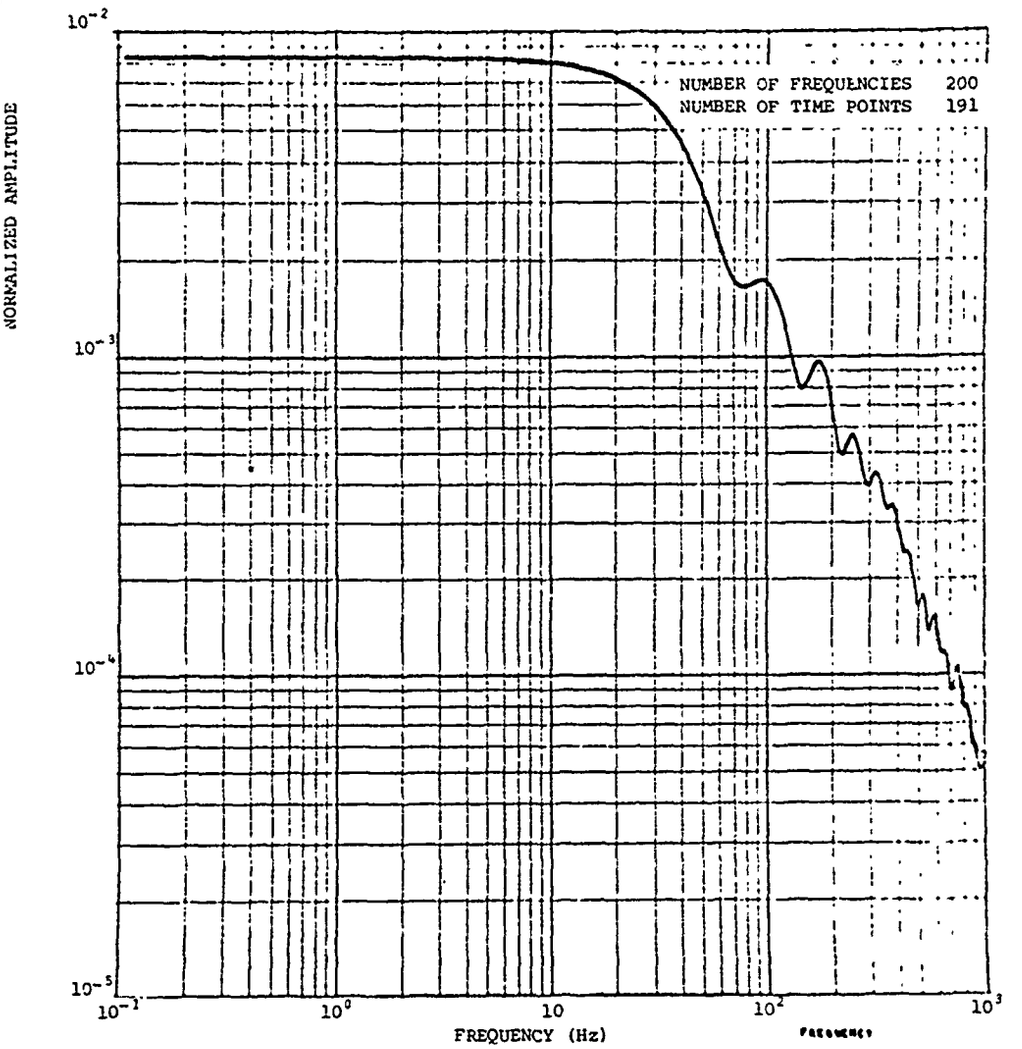


Figure 4. Spectrum of Signal

DISTRIBUTION:

L. Rorden
C. Moore
T. Kennedy
Lt. Cmdr. L. Piper
Lt. John Gallamore
B. Hartenbaum
Coye Vincent
D. Day
F. Hanes
Lt. Col. D. Burgess

DISTRIBUTION LIST

DEPARTMENT OF DEFENSE

Defense Documentation Center
Cameron Station
12 cy ATTN: TC

Director, Defense Nuclear Agency
ATTN: TISI
ATTN: DDST
ATTN: SPSS, Dr. Sevin
ATTN: SPAS
ATTN: SPTD, Captain Summa
ATTN: TITL
2 cy ATTN: SPSS, T. Kennedy

Commander
Field Command, Defense Nuclear Agency
ATTN: FCTMO
ATTN: FCT, Col Yavra
ATTN: FCTME
ATTN: FCPR
2 cy ATTN: FCTMO, LCDR R. L. Piper

Chief
Livermore Div., Fld. Command, DNA
ATTN: FCPRL
ATTN: Doc. Control

Chief, Test Construction Div.
Field Command Test Directorate
ATTN: NTS, Joe LaComb

Under Sec'y of Def. for Rsch. & Engrg.
ATTN: S&SS (OS)
ATTN: AE

DEPARTMENT OF THE ARMY

Commander
Harry Diamond Laboratories
ATTN: DELHD-NP

Director
US Army Engr. Waterways Exper. Sta.
ATTN: Don Day
ATTN: Research Center Library
ATTN: F. Hanes
ATTN: L. Ingram

DEPARTMENT OF THE NAVY

Officer-in-Charge
Naval Surface Weapons Center
ATTN: Code WA501, Navy Nuc. Prgms. Ofc.

Officer-in-Charge
Civil Engineering Laboratory
Naval Construction Battalion Center
ATTN: L31

DEPARTMENT OF THE AIR FORCE

AF Weapons Laboratory, AFSC
ATTN: SUL
2 cy ATTN: DED-I

DEPARTMENT OF ENERGY

Los Alamos Scientific Laboratory
ATTN: Reports Library

University of California
Lawrence Livermore Laboratory
2 cy ATTN: David Oakley

OTHER GOVERNMENT AGENCY

Dept. of Commerce
National Bureau of Standards
ATTN: Sec. Officer for P. S. Lederer,
Chief, Components & Applications Section

DEPARTMENT OF DEFENSE CONTRACTORS

Agbabian Associates
ATTN: Doc. Control
ATTN: C. F. Bagge

The Boeing Company
ATTN: James Wooster
ATTN: Robert Holmes

DEVELCO, Inc.
ATTN: L. H. Rorden
ATTN: T. C. Moore
ATTN: D. H. Nitta
ATTN: C. Kwong
ATTN: A. Weston
ATTN: E. Hutchins

Electromechanical Sys. of New Mexico, Inc.
ATTN: R. A. Shunk

General Electric Company
TEMPO-Center for Advanced Studies
ATTN: DASIAC

Merritt CASES, Inc.
ATTN: J. L. Merritt

Pacifica Technology
ATTN: R. Bjork

Physics International Company
ATTN: C. Vincent

R & D Associates
ATTN: C. Knowles
ATTN: H. L. Brode
ATTN: H. Cooper

SRI International
ATTN: George Abrahamson
ATTN: D. Keough